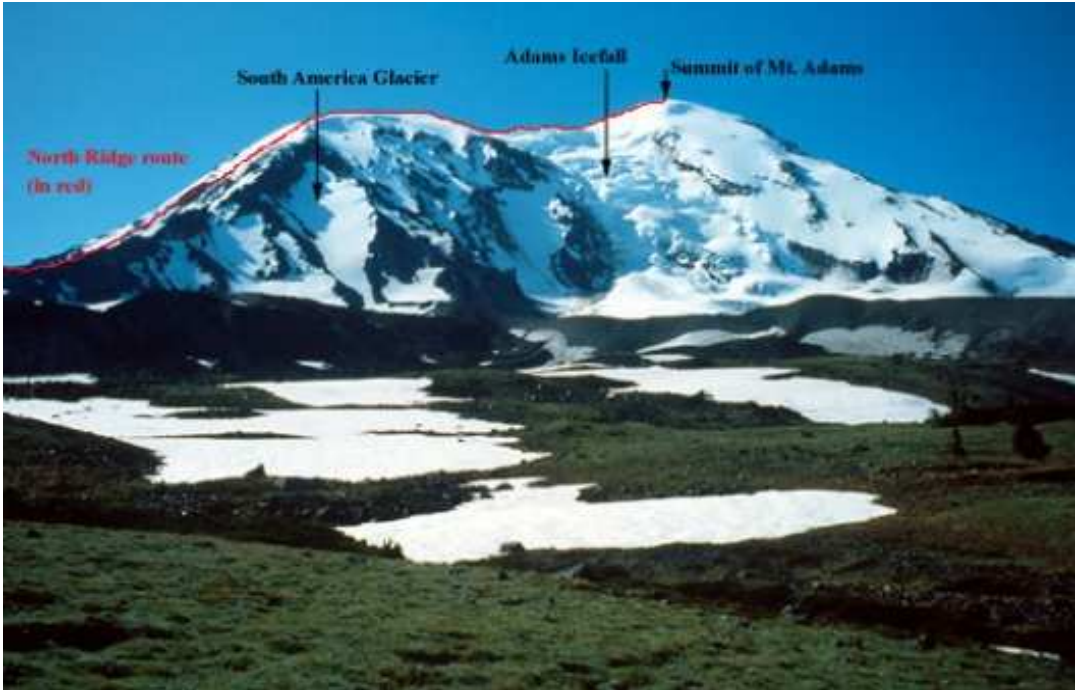


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DEPARTMENT
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Intel Corporation
2200 Mission College Blvd.
P.O. BOX 58119
Santa Clara, CA 95052-8119

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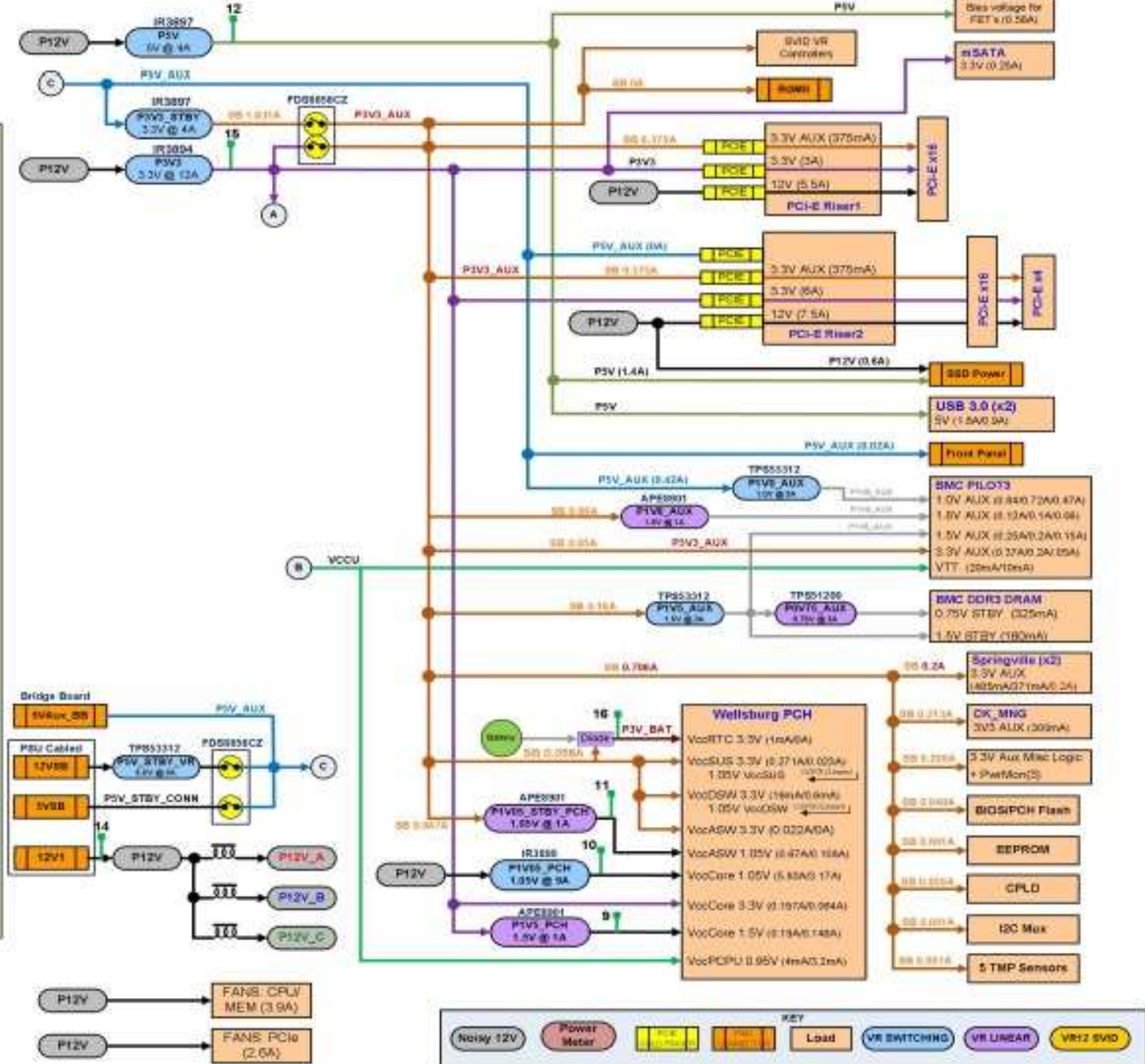
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81	BMC - PILOT III (3/6)																																																																																																																																																																																																																																																																
82	BMC - PILOT III (4/6)																																																																																																																																																																																																																																																																
83	BMC - PILOT III (5/6)																																																																																																																																																																																																																																																																
84	BMC - PILOT III (6/6)																																																																																																																																																																																																																																																																
85	BMC DECOUPLING																																																																																																																																																																																																																																																																
86	BMC CONFIGURATION																																																																																																																																																																																																																																																																
87	RGMII																																																																																																																																																																																																																																																																
88	BMC DDR3 MEMORY																																																																																																																																																																																																																																																																
89	BMC DDR3 MEMORY																																																																																																																																																																																																																																																																
90	BMC FLASH/RMM4 LITE																																																																																																																																																																																																																																																																
91	BMC JTAG/PECI																																																																																																																																																																																																																																																																
92	BMC MISC																																																																																																																																																																																																																																																																
93	BMC SPKR/USB																																																																																																																																																																																																																																																																
94	BMC VIDEO																																																																																																																																																																																																																																																																
95	BMC SERIAL PORT																																																																																																																																																																																																																																																																
96	BMC AVIN																																																																																																																																																																																																																																																																
97	BMC TEMP SENSORS																																																																																																																																																																																																																																																																
98	BMC TEMP SENSORS																																																																																																																																																																																																																																																																
99	BMC SGPIO (1 OF 2)																																																																																																																																																																																																																																																																
100	BMC SGPIO (2 OF 2)																																																																																																																																																																																																																																																																
101	NODE POWER BOARD CONNECTOR																																																																																																																																																																																																																																																																
102	SYS FAN CONNECTORS																																																																																																																																																																																																																																																																
103	SMBUS LEVEL-SHIFTER																																																																																																																																																																																																																																																																
104	SMBUS MUX																																																																																																																																																																																																																																																																
105	SMBUS ISOLATION																																																																																																																																																																																																																																																																
106	SPRINGVILLE 0 (1 OF 2)																																																																																																																																																																																																																																																																
107	SPRINGVILLE 0 (2 OF 2)																																																																																																																																																																																																																																																																
108	SPRINGVILLE 1 (1 OF 2)																																																																																																																																																																																																																																																																
109	SPRINGVILLE 1 (2 OF 2)																																																																																																																																																																																																																																																																
110	RJ45 CONNECTOR																																																																																																																																																																																																																																																																
111	FRONT PANEL HEADER/LEDS																																																																																																																																																																																																																																																																
112	BRIDGE BOARD																																																																																																																																																																																																																																																																
113	POWER SEQUENCING CPLD																																																																																																																																																																																																																																																																
114	SIDEBAND LEVEL-TRANSLATORS 1/2																																																																																																																																																																																																																																																																
115	SIDEBAND LEVEL-TRANSLATORS 2/2																																																																																																																																																																																																																																																																
116	POWER CONNECTORS																																																																																																																																																																																																																																																																
117	P3V3_STBY VR																																																																																																																																																																																																																																																																
118	P5V_STBY VR																																																																																																																																																																																																																																																																
119	P5V_STBY SWITCH																																																																																																																																																																																																																																																																
120	P3V3_AUX SWITCH																																																																																																																																																																																																																																																																
Thu Nov 17 15:13:13 2016																																																																																																																																																																																																																																																																	
INDEX 1				DEPARTMENT BESD				Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119				SIZE	CODE	DOCUMENT NUMBER		REV																																																																																																																																																																																																																																																	
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Thu Nov 17 15:13:14 2016

POWER SEQUENCE DIAGRAM LAST UPDATED: 15' WW02

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34649

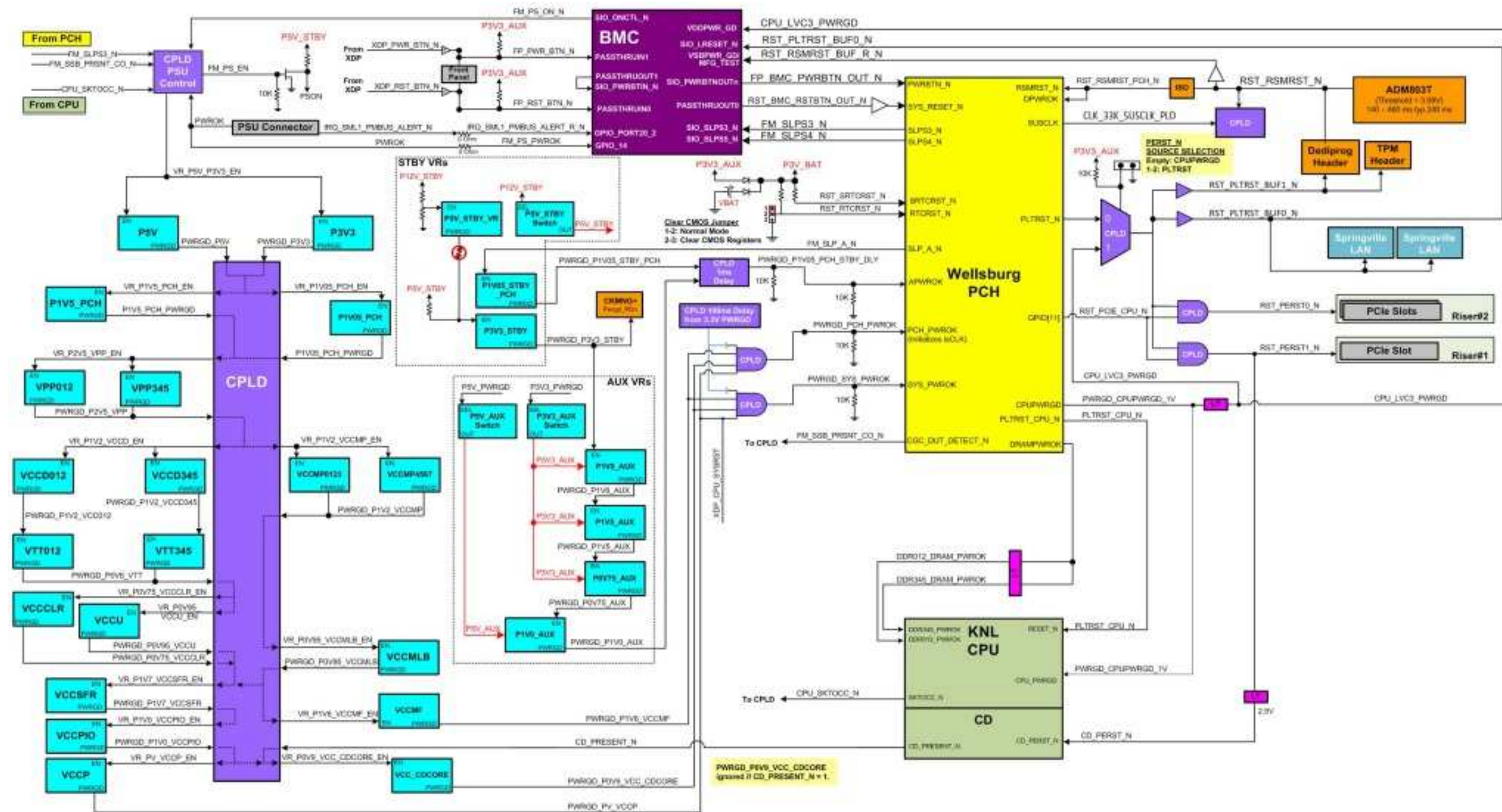
DOCUMENT NUMBER
G9428608

REV
3. 1.3

SCALE:

DO NOT SCALE DRAWING

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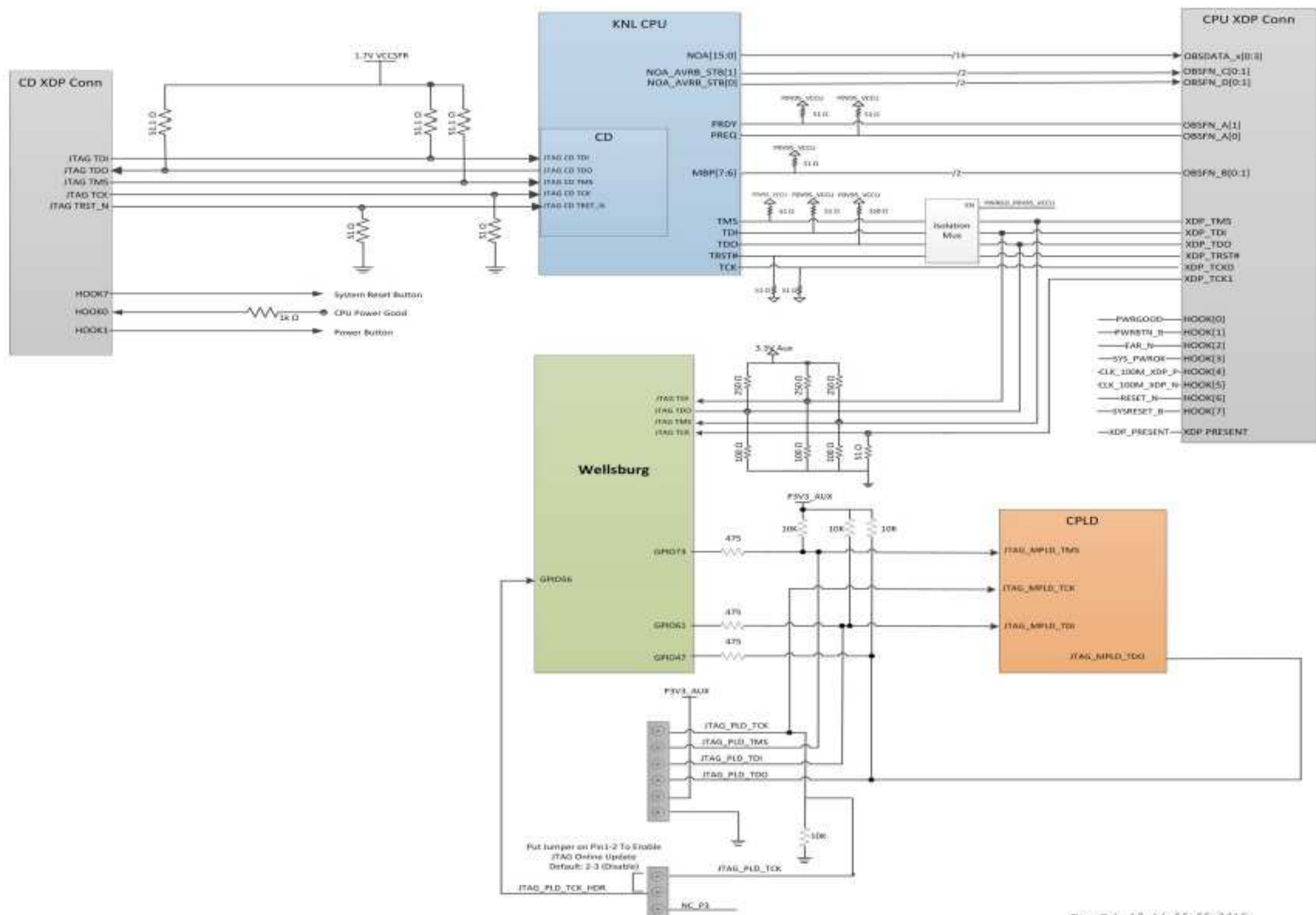


4

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2

1



Tue Feb 17 14:23:55 2015

Thu Nov 17 15:13:15 2016

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JTAG DIAGRAMS

LAST UPDATED: 15' WW05

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3.1.3

SCALE:

DO NOT SCALE DRAWING

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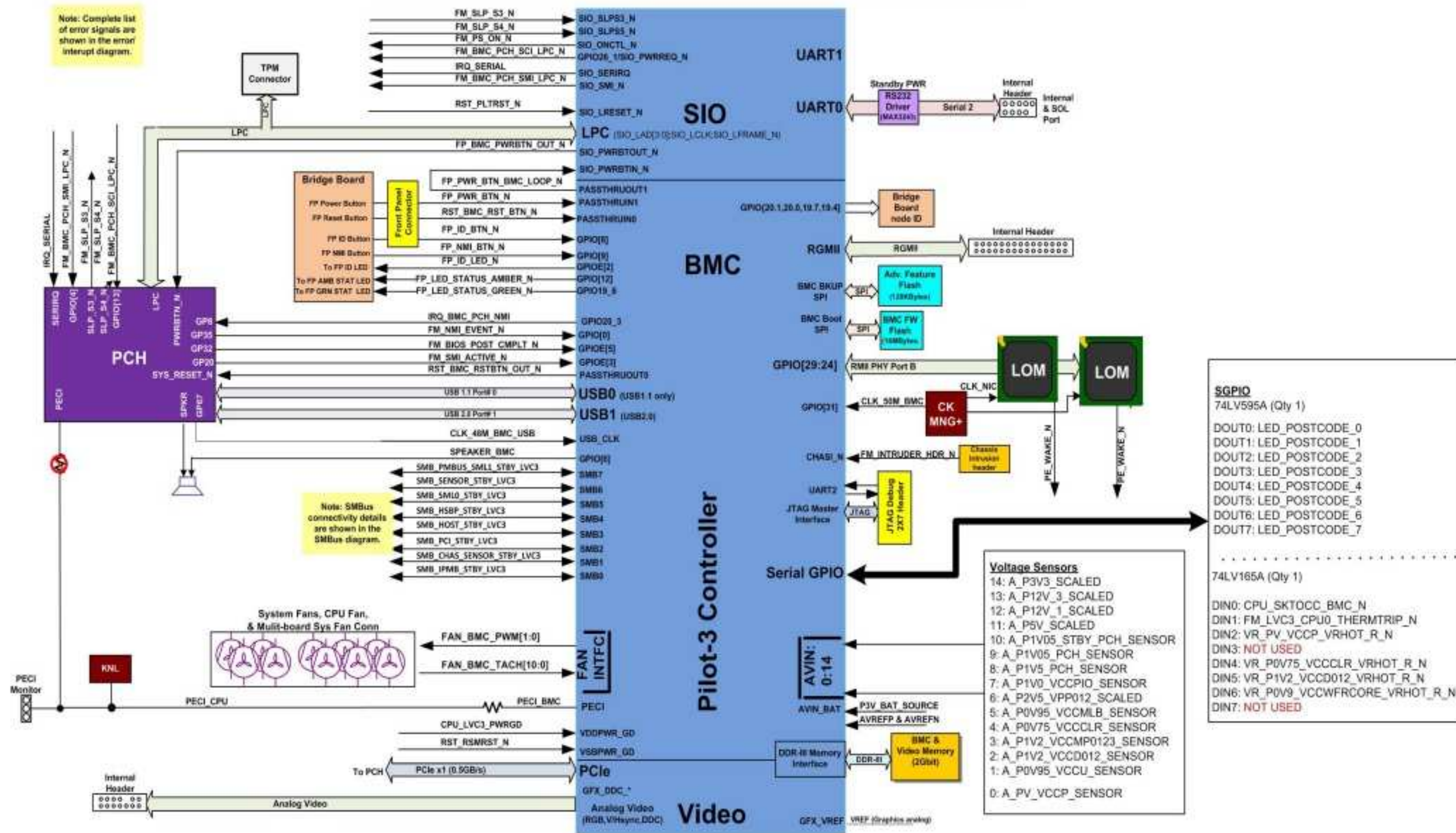
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3

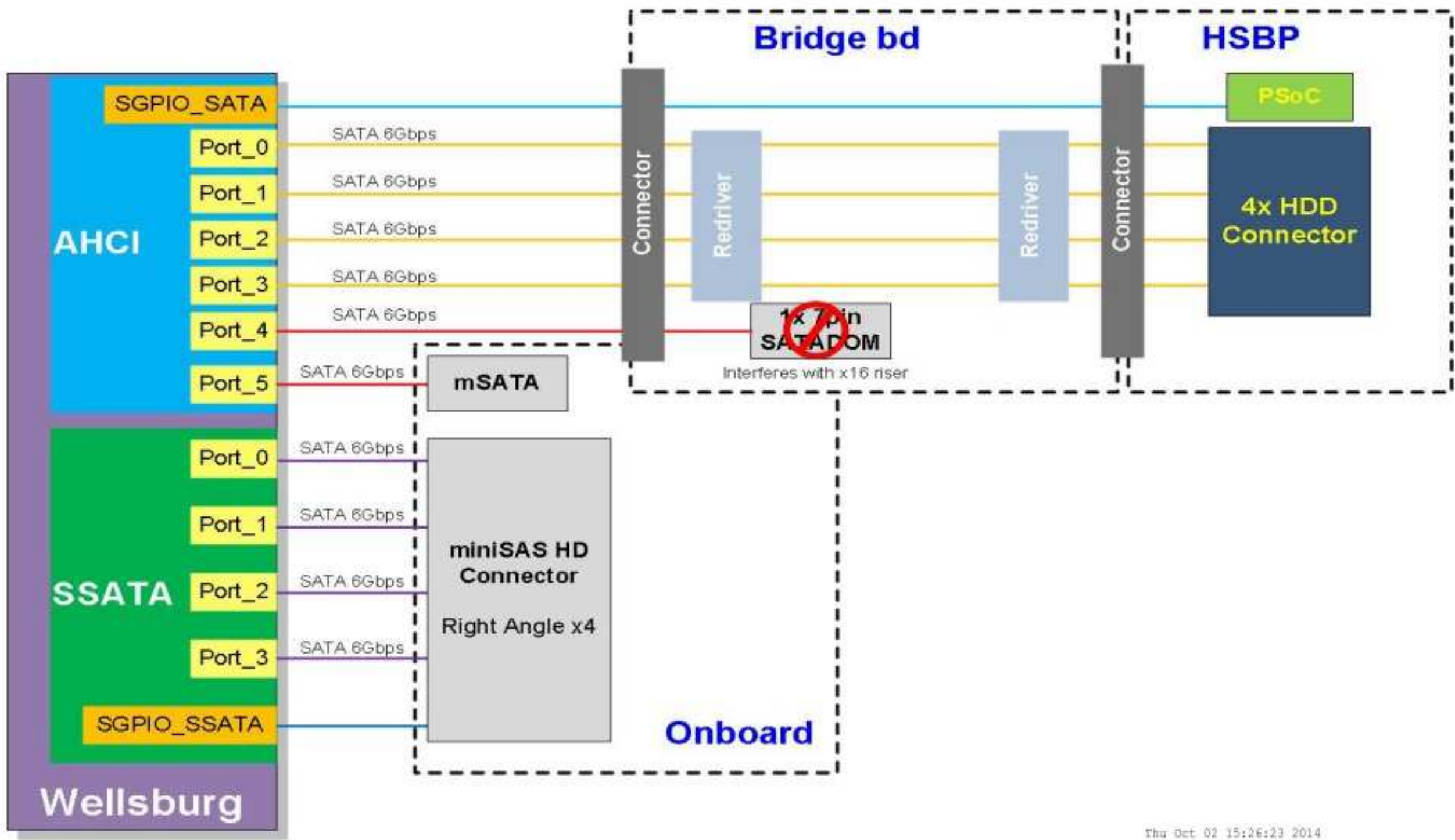
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1

Note: Complete list of error signals are shown in the error interrupt diagram.

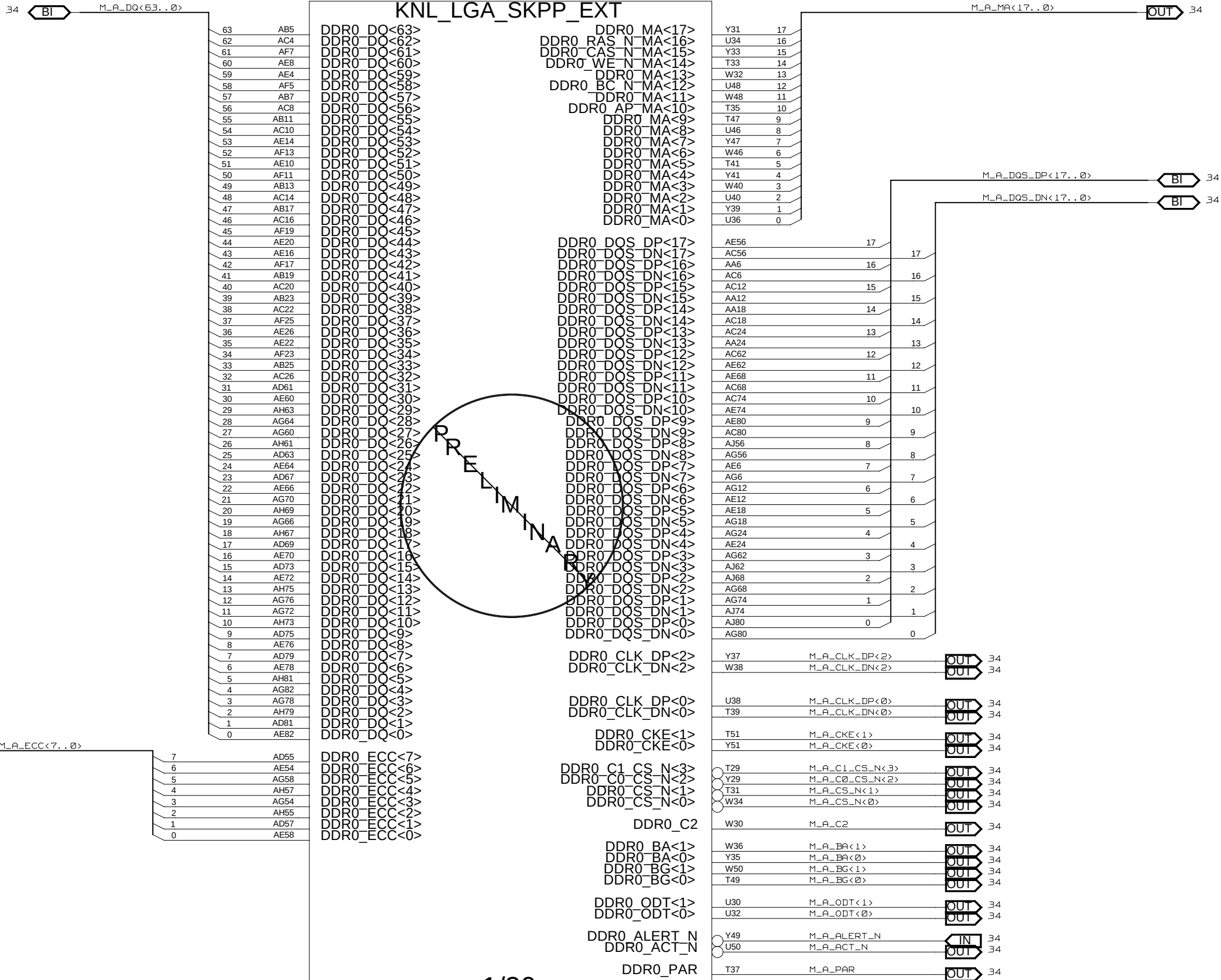


SATA Block Diagram



Thu Oct 02 15:26:23 2014

Thu Nov 17 15:13:16 2016



ROOM: KNL

KNL LGA DDR CH0

1/30

G7B0B1-001

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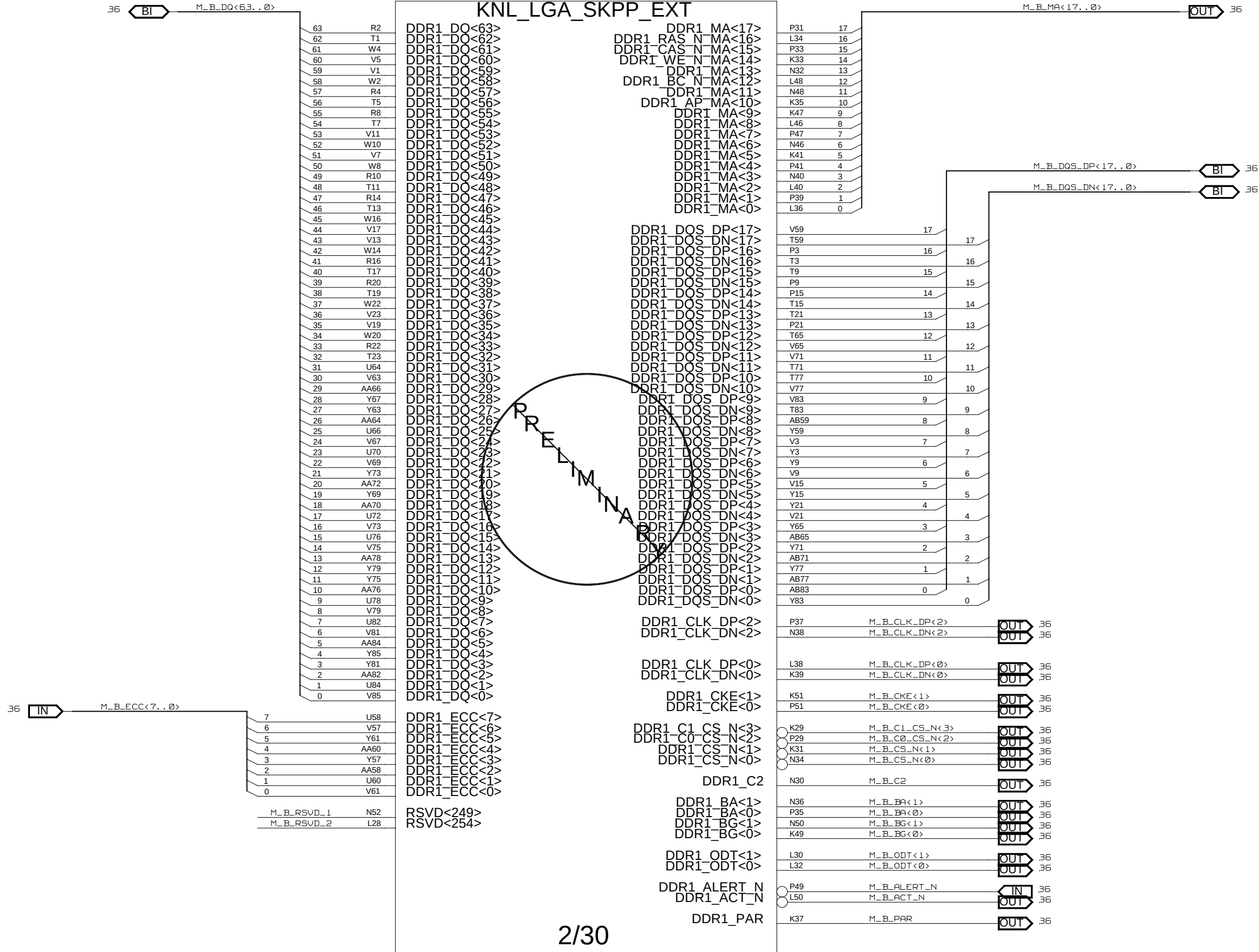
REV
.3.13

SCALE:

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SHEET 14 OF 167

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ROOM: KNL

KNL LGA DDR CH1

G7B0B1-001

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CODE
34649

DOCUMENT NUMBER
G9428608

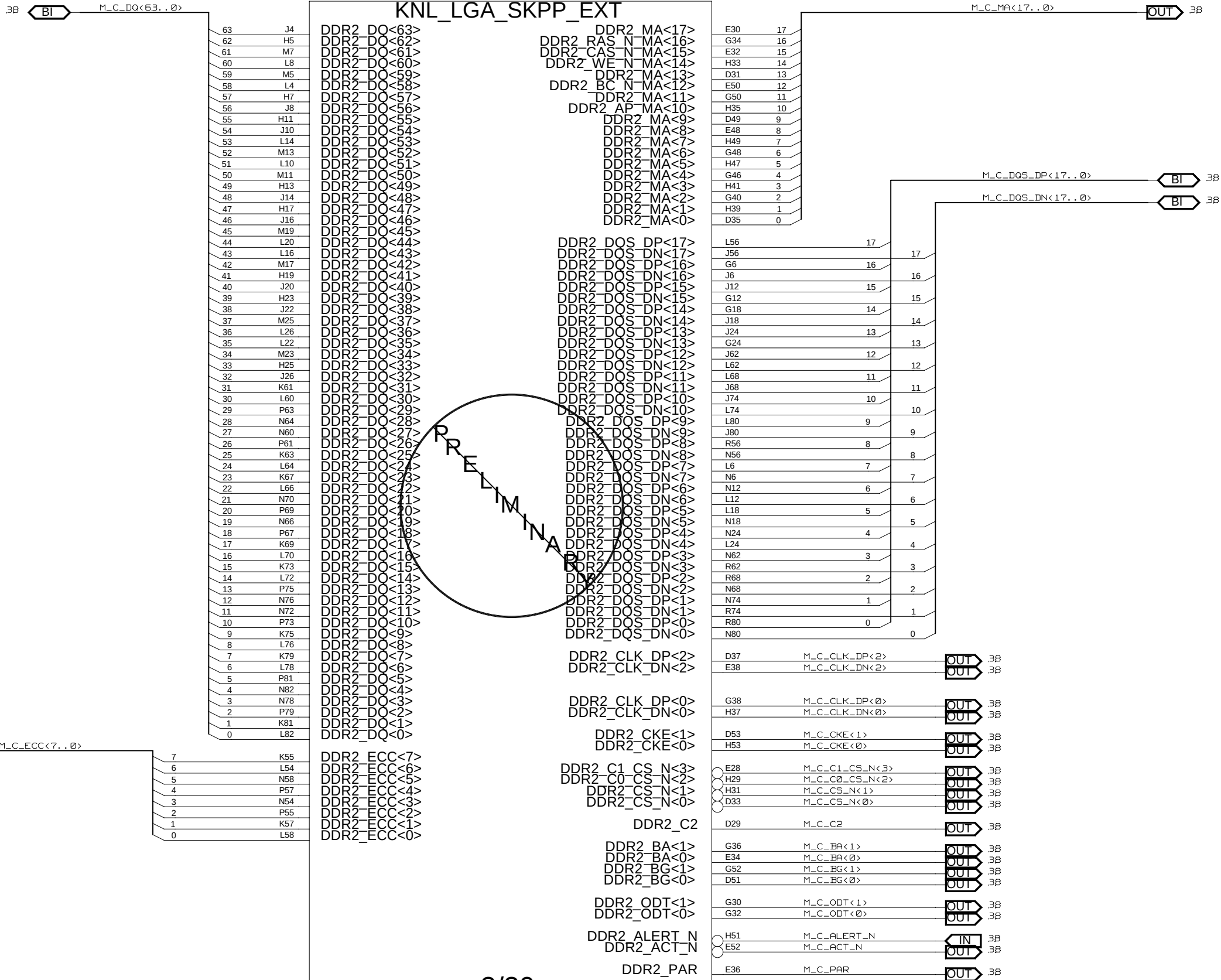
REV
.3.13

SCALE:

DO NOT SCALE DRAWING

SHEET 15 OF 167

Thu Nov 17 15:19:14 2016



ROOM: KNL

KNL LGA DDR CH2

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DOCUMENT NUMBER

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REV

3.13

SCALE:

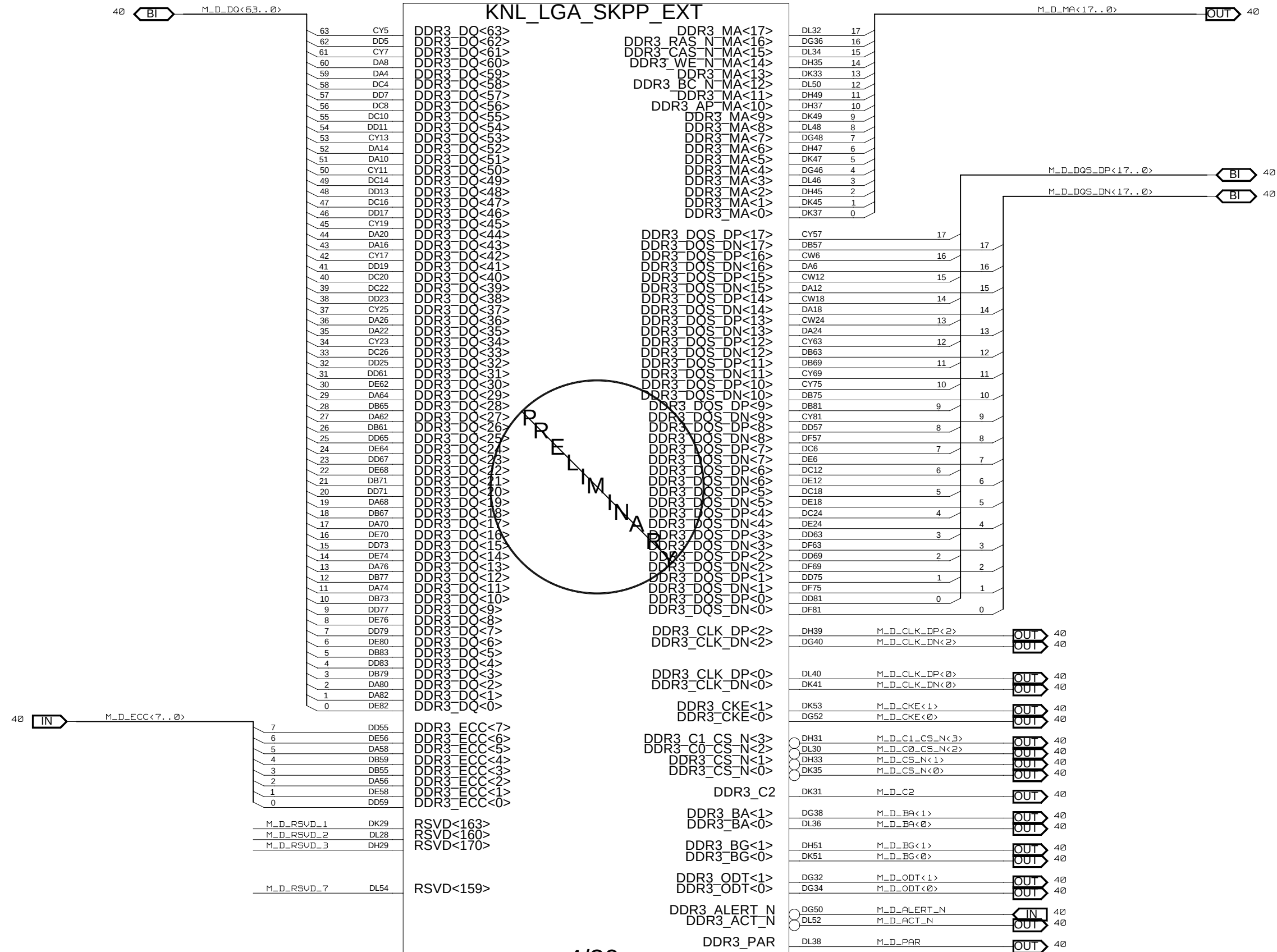
DO NOT SCALE DRAWING

SHEET 16 OF 167

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U1 EMPTY



ROOM: KNL

KNL LGA DDR CH.3

G78081-001

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DOCUMENT NUMBER

G9428608

REV

3.13

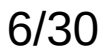
SCALE:

DO NOT SCALE DRAWING

SHEET 17 OF 167

Thu Nov 17 15:19:14 2016

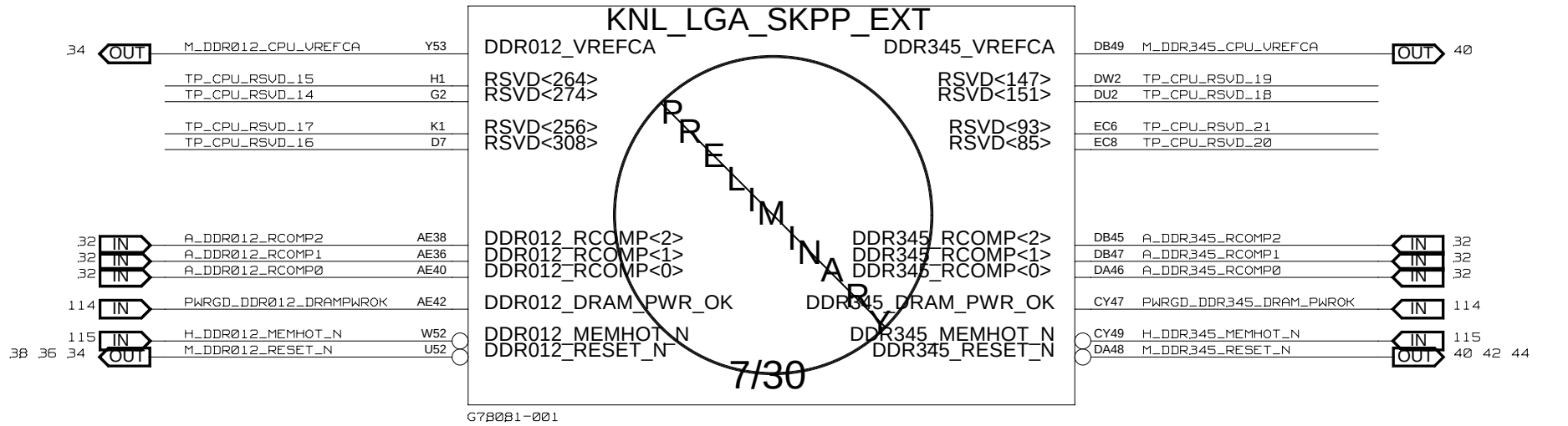
KNL_LGA_SKPP_EXT



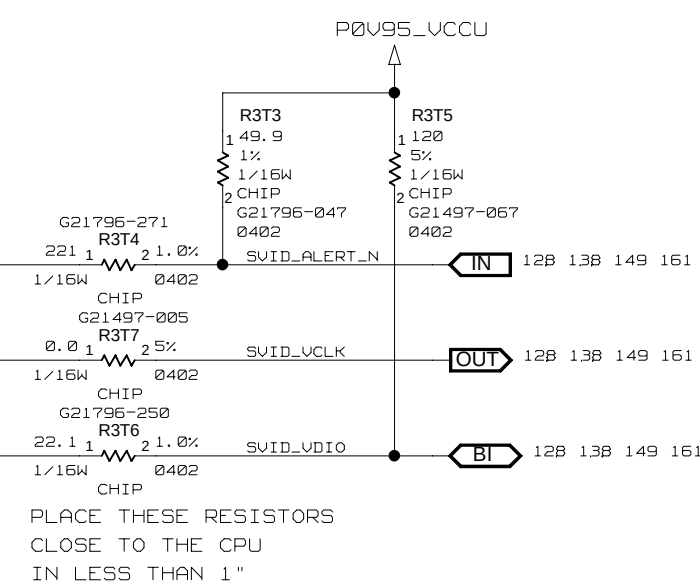
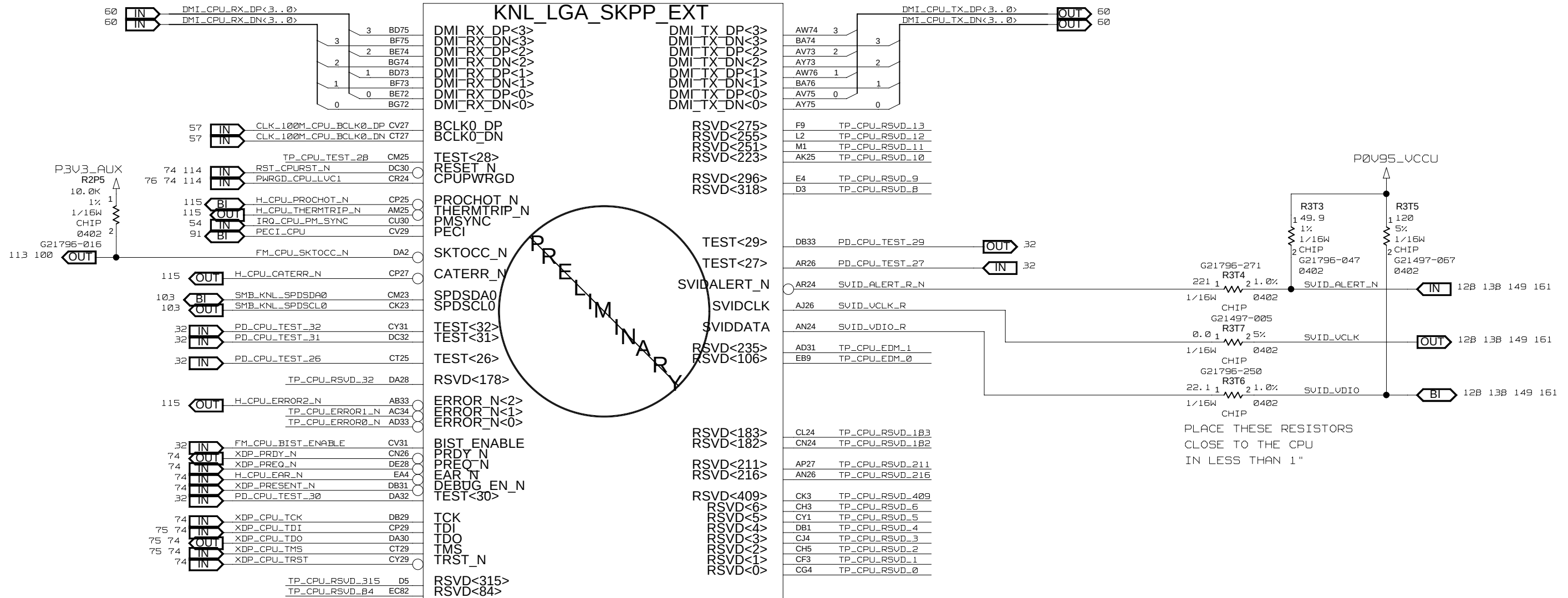
1

KNL LGA DDR CH5

U1 EMPTY



U1 EMPTY



ROOM: KNL

KNL LGA DDR-DMI-MISC/I/0

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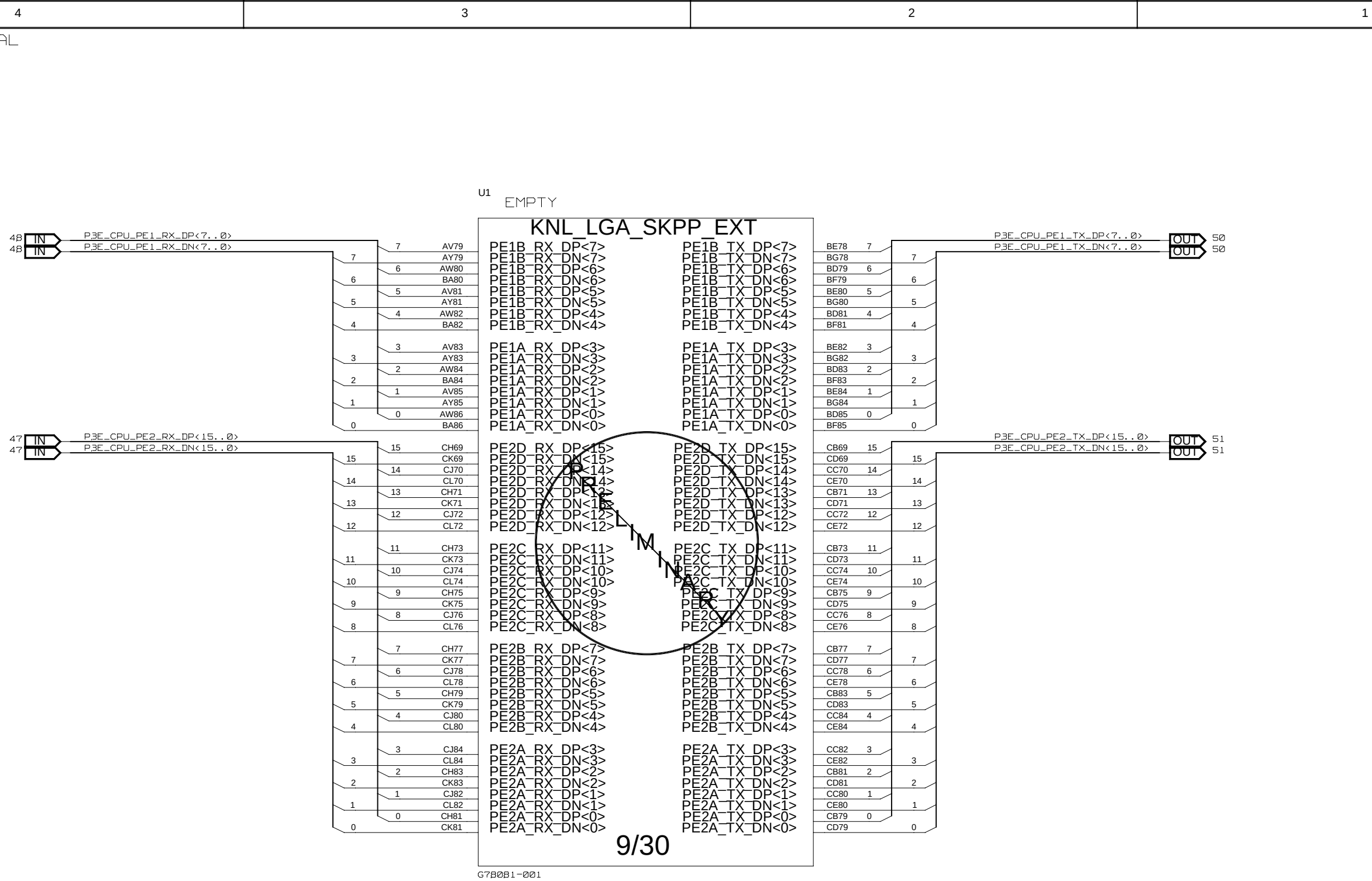
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SCALE:

DO NOT SCALE DRAWING

SHEET 20 OF 167

Thu Nov 17 15:19:15 2016

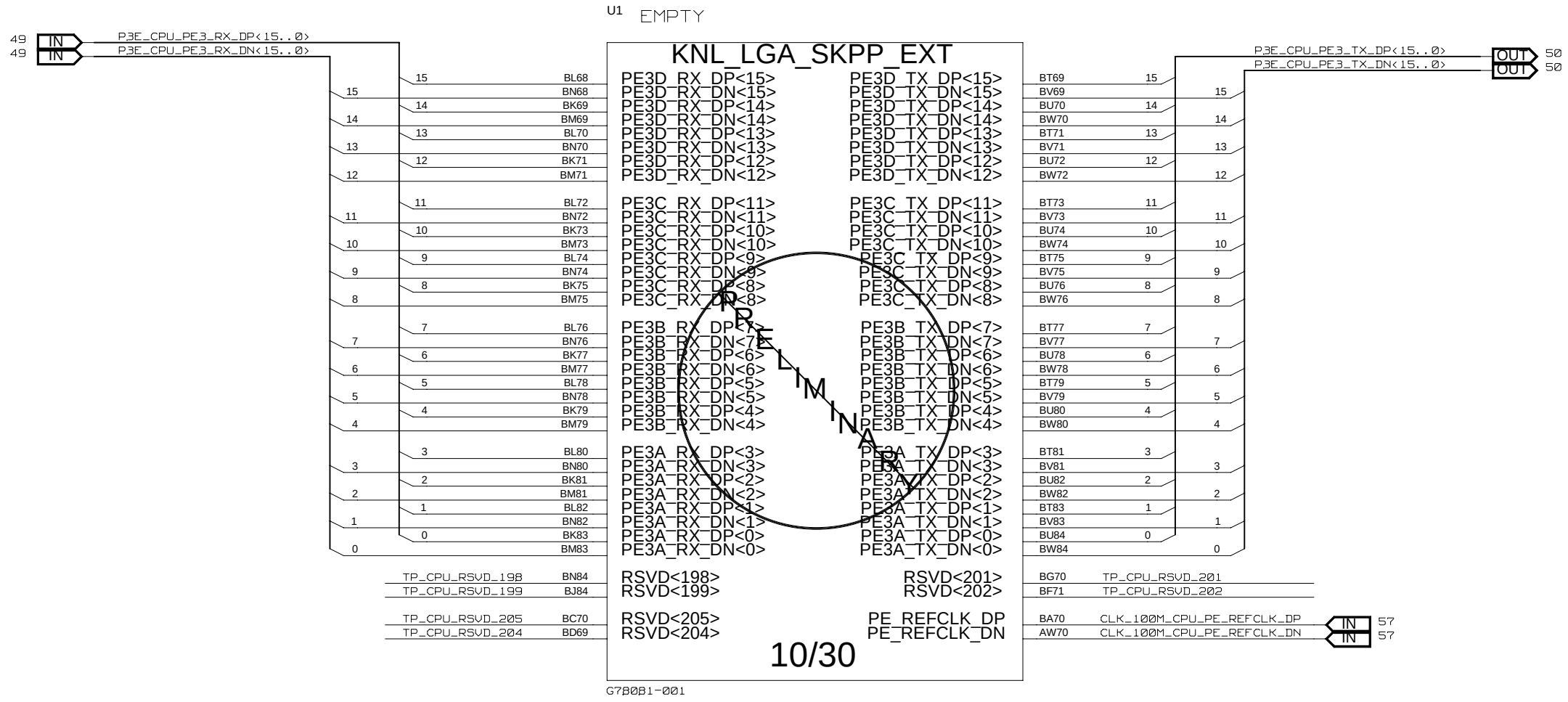


ROOM: KNL

KNL LGA PCIE PORTS 1/2

Thu Nov 17 15:19:15 2016

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
CBED	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	G9428608	.3.1.3
SCALE:		DO NOT SCALE DRAWING			SHEET 21 OF 167

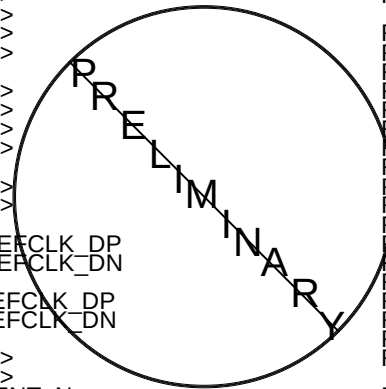


ROOM: KNL

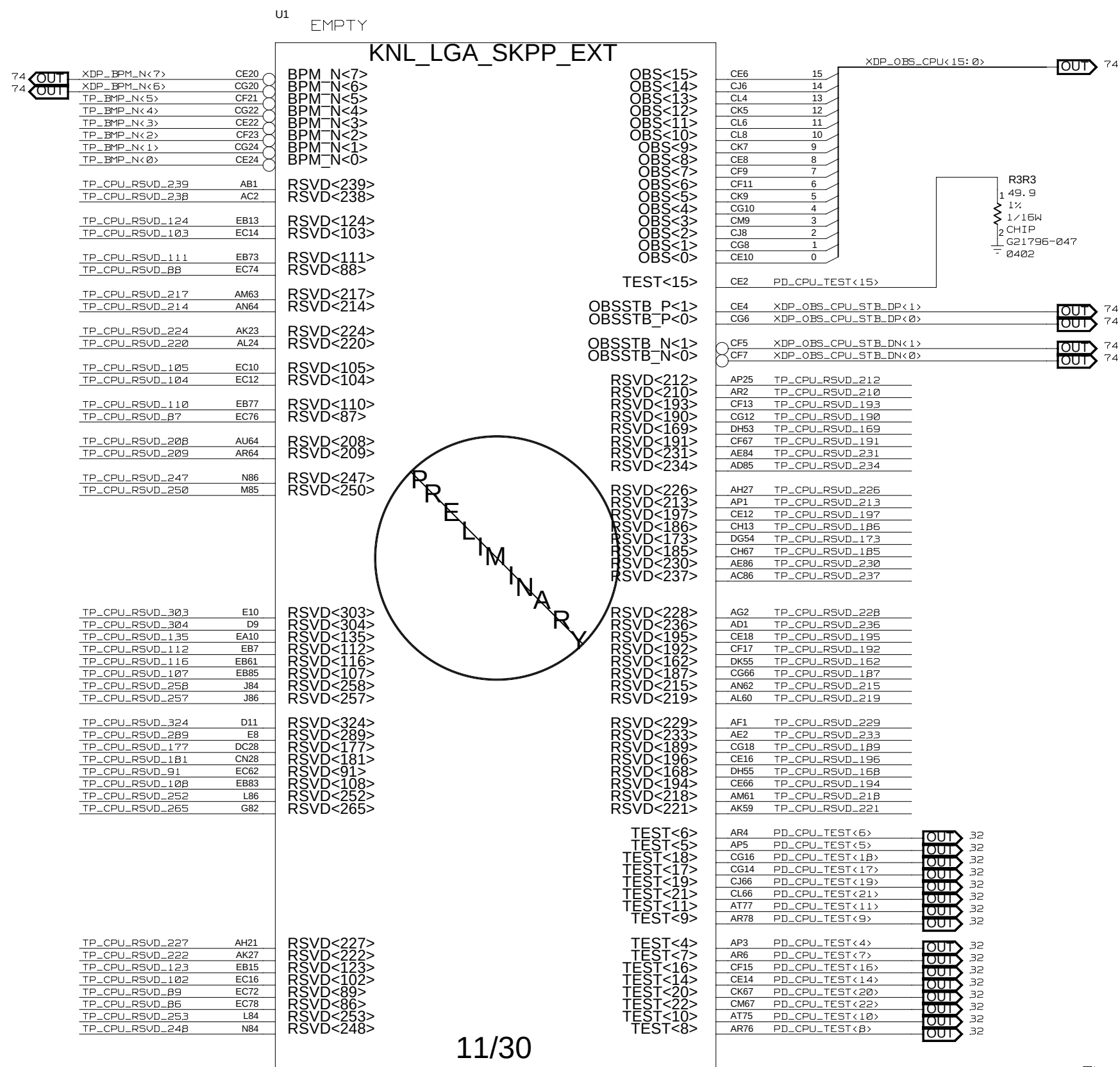
KNL LGA PCIE PORT .3

Thu Nov 17 15:19:16 2016

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
CBED	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	G9428608	.3.1.3
SCALE:		DO NOT SCALE DRAWING			SHEET 22 OF 167



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ROOM: KNL

KNL LGA MISC

4

3

2

1

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DOCUMENT NUMBER

G9428608

REV

3.13

SCALE:

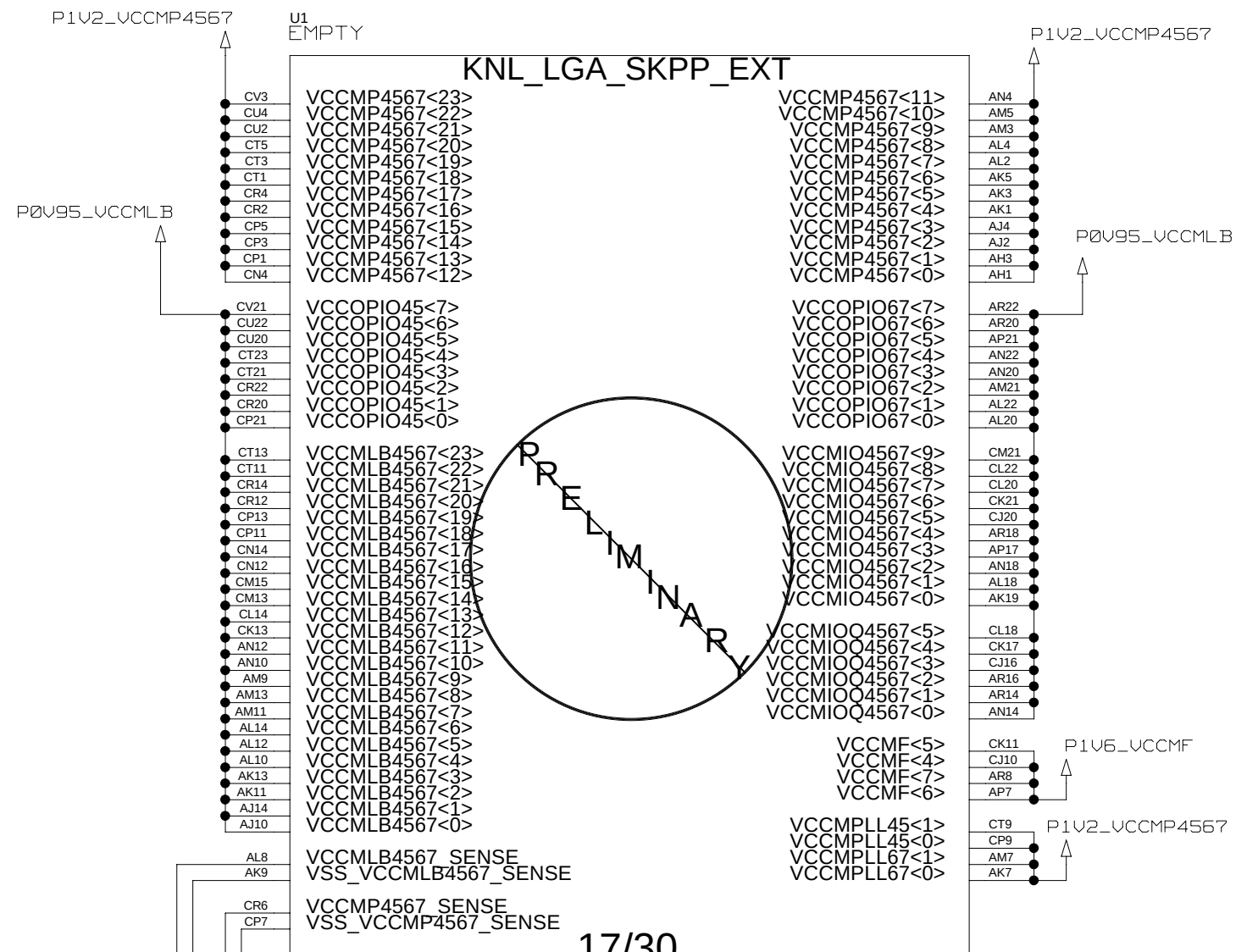
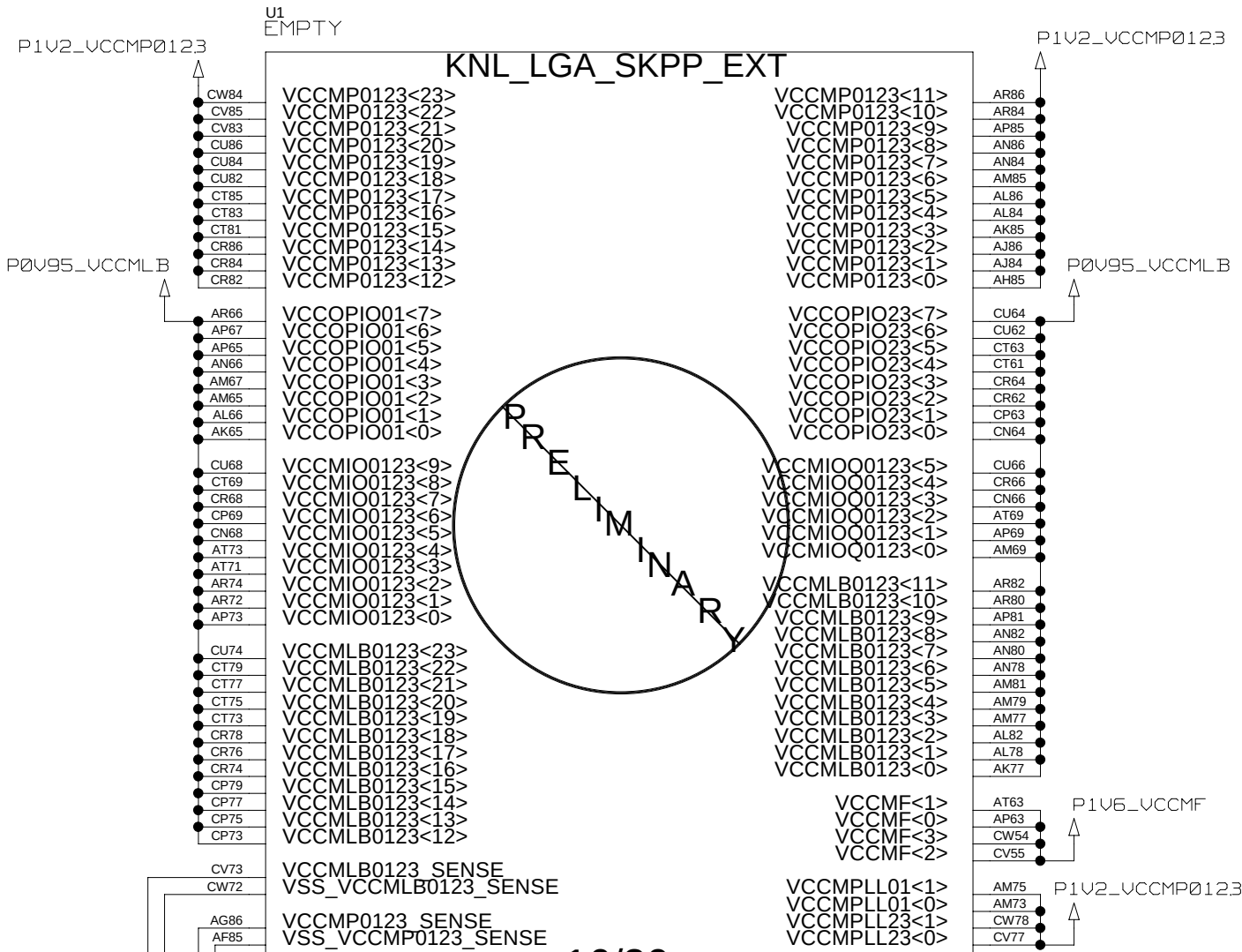
DO NOT SCALE DRAWING

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11/30

G78081-001



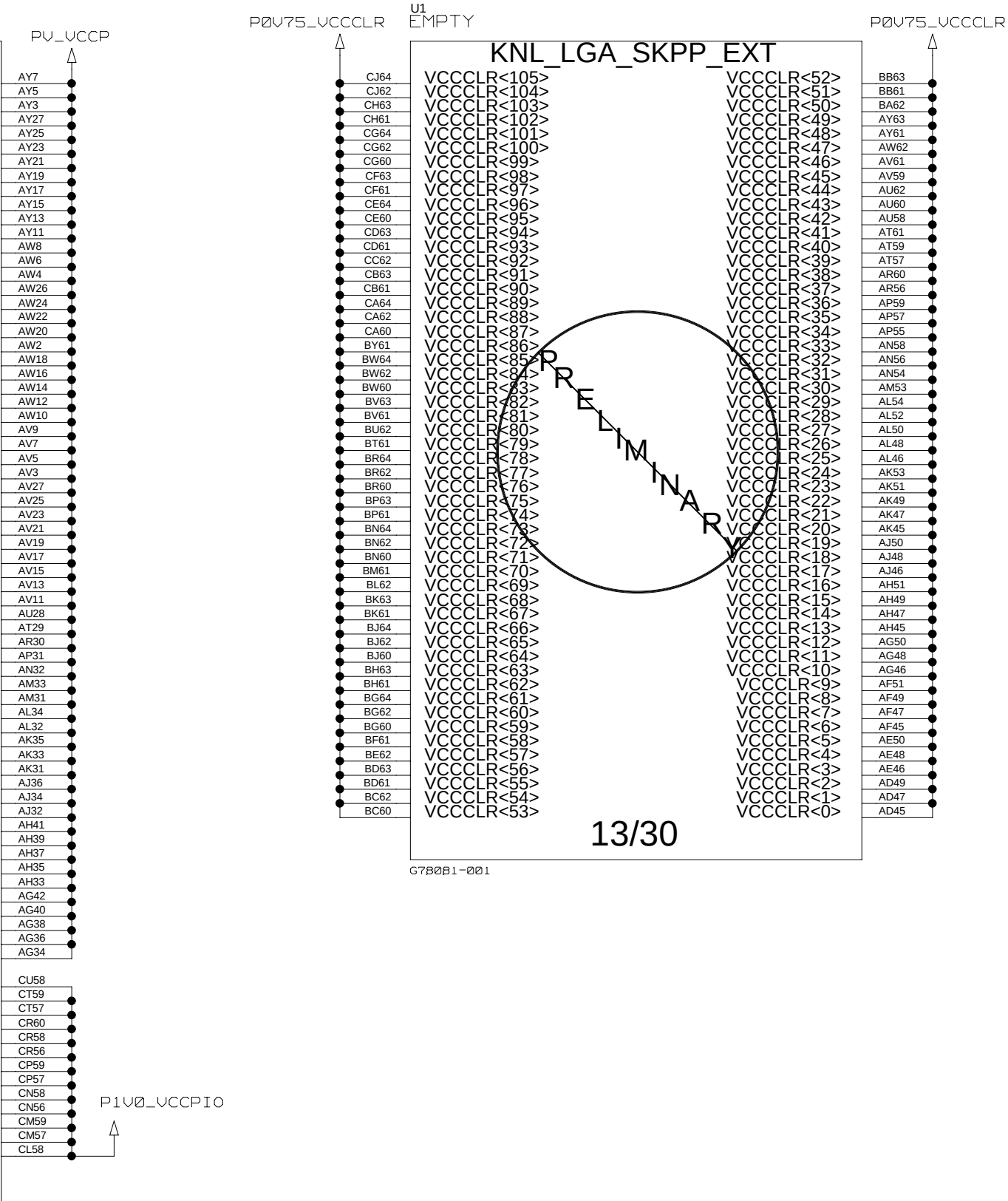
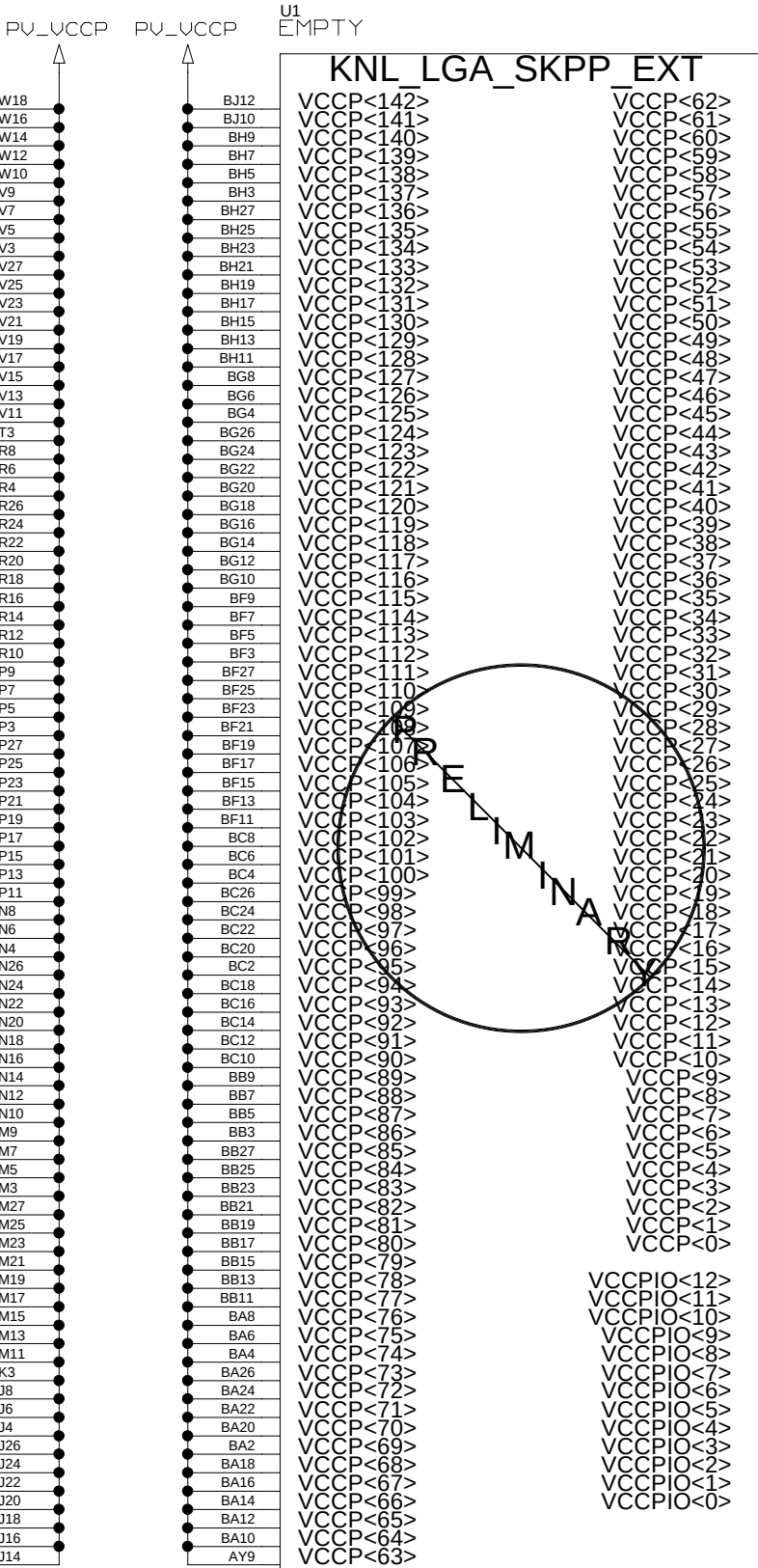
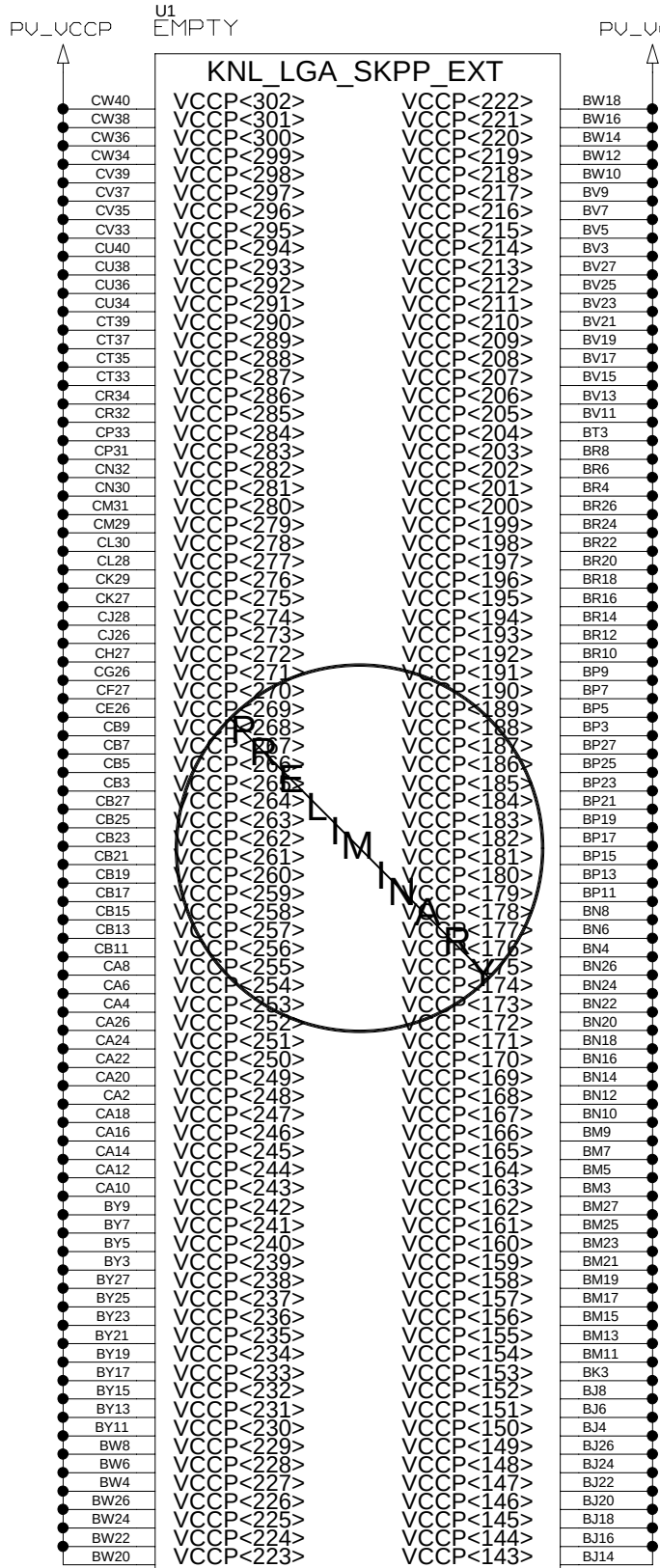
ROOM: KNL

KNL LGA POWER (1 OF 5)

Thu Nov 17 15:19:16 2016

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
CBED	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	G9428608	.3.13
		SCALE:	DO NOT SCALE DRAWING		SHEET 25 OF 167

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ROOM: KNL

KNL LGA POWER (2 OF 5)

Thu Nov 17 15:19:17 2016

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SIZE

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CODE

34649

DOCUMENT NUMBER

G9428608

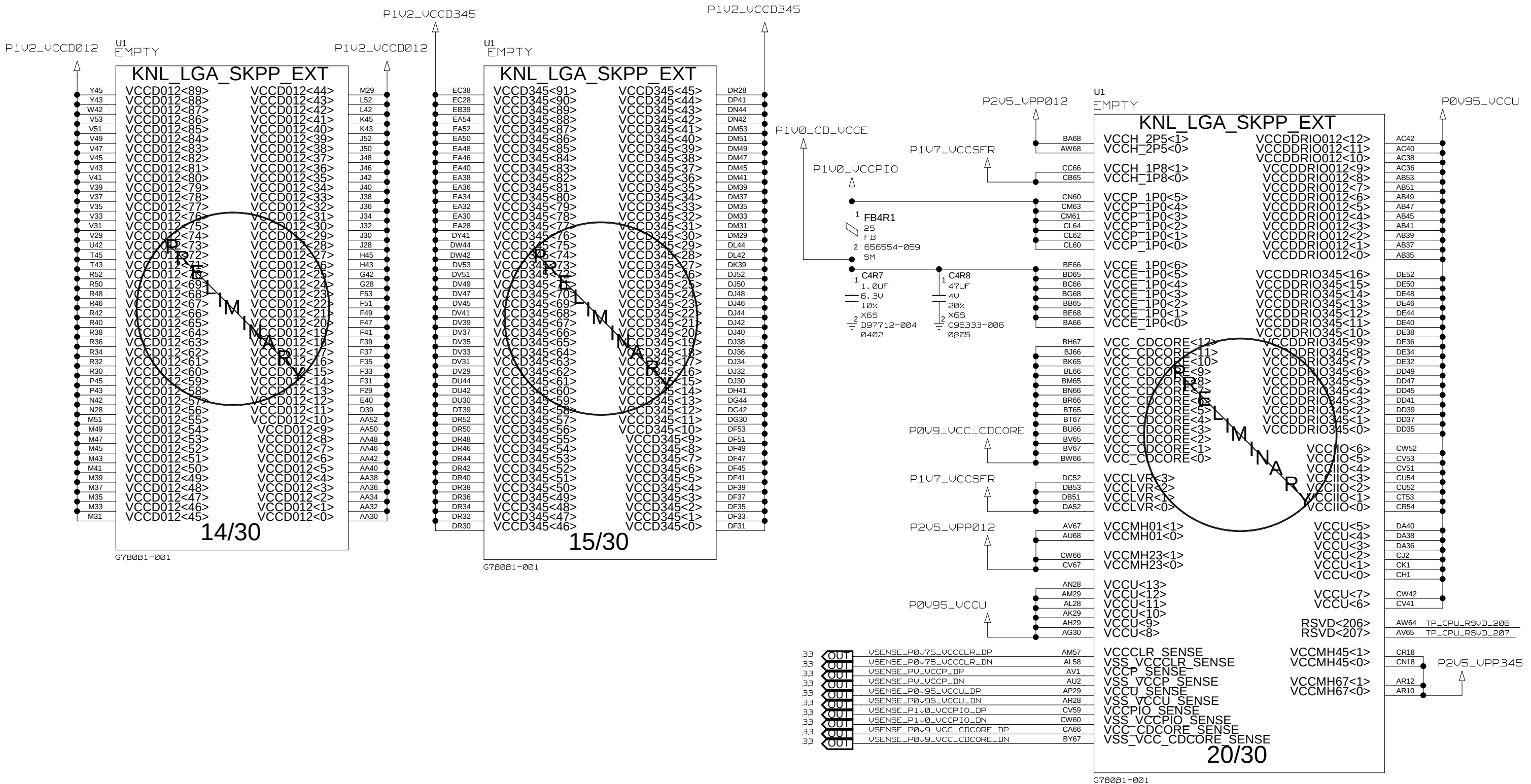
REV

3.13

SCALE:

DO NOT SCALE DRAWING

SHEET 26 OF 167



ROOM: KNL

KNL LGA POWER (3 OF 5)

Thu Nov 17 15:19:17 2016

DEPARTMENT

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DOCUMENT NUMBER

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REV

3.13

SCALE:

DO NOT SCALE DRAWING

SHEET 27 OF 167

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U1
EMPTY

KNL_LGA_SKPP_EXT

Y7	VSS<1167>	VSS<1087>	AP11
Y5	VSS<1166>	VSS<1086>	AN8
Y27	VSS<1165>	VSS<1085>	AN76
Y25	VSS<1164>	VSS<1084>	AN74
Y23	VSS<1163>	VSS<1083>	AN68
Y19	VSS<1162>	VSS<1082>	AN60
Y17	VSS<1161>	VSS<1081>	AN6
Y13	VSS<1160>	VSS<1080>	AN30
Y11	VSS<1159>	VSS<1079>	AM83
Y1	VSS<1158>	VSS<1078>	AM59
W86	VSS<1157>	VSS<1077>	AM55
W84	VSS<1156>	VSS<1076>	AM27
BB81	VSS<1155>	VSS<1075>	AM23
BB79	VSS<1154>	VSS<1074>	AM19
BB77	VSS<1153>	VSS<1073>	AM1
BB75	VSS<1152>	VSS<1072>	AL80
BB73	VSS<1151>	VSS<1071>	AL76
BB71	VSS<1150>	VSS<1070>	AL74
BA78	VSS<1149>	VSS<1069>	AL64
BA72	VSS<1148>	VSS<1068>	AL62
BA64	VSS<1147>	VSS<1067>	AL6
BA60	VSS<1146>	VSS<1066>	AL56
AY77	VSS<1145>	VSS<1065>	AL30
AY71	VSS<1144>	VSS<1064>	AL26
AY69	VSS<1143>	VSS<1063>	AK83
AW78	VSS<1142>	VSS<1062>	AK81
AW72	VSS<1141>	VSS<1061>	AK79
AW60	VSS<1140>	VSS<1060>	AK75
AV71	VSS<1139>	VSS<1059>	AK69
AV69	VSS<1138>	VSS<1058>	AK67
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AU80	VSS<1133>	VSS<1053>	AK21
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AT67	VSS<1110>	VSS<1030>	AH59
AT5	VSS<1109>	VSS<1029>	AH5
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AT21	VSS<1104>	VSS<1024>	AH15
AT19	VSS<1103>	VSS<1023>	AH13
AT17	VSS<1102>	VSS<1022>	AH11
AT15	VSS<1101>	VSS<1021>	AG84
AT13	VSS<1100>	VSS<1020>	AG8
AT1	VSS<1099>	VSS<1019>	AG4
AR68	VSS<1098>	VSS<1018>	AG32
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AR58	VSS<1096>	VSS<1016>	AG26
AP9	VSS<1095>	VSS<1015>	AG22
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AP19	VSS<1089>	VSS<1009>	AF81
AP13	VSS<1088>	VSS<1008>	AF79

21/30

G7B0B1-001

U1
EMPTY

KNL_LGA_SKPP_EXT

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AF69	VSS<1003>	VSS<923>	P25
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AF65	VSS<1001>	VSS<921>	P19
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W80	VSS<998>	VSS<918>	P11
W78	VSS<997>	VSS<917>	P1
W76	VSS<996>	VSS<916>	N8
W74	VSS<995>	VSS<915>	N4
W72	VSS<994>	VSS<914>	N26
W70	VSS<993>	VSS<913>	N22
W68	VSS<992>	VSS<912>	N20
W66	VSS<991>	VSS<911>	N2
W64	VSS<990>	VSS<910>	N16
W62	VSS<989>	VSS<909>	N14
W60	VSS<988>	VSS<908>	N10
W6	VSS<987>	VSS<907>	M9
W58	VSS<986>	VSS<906>	M83
W56	VSS<985>	VSS<905>	M81
W52	VSS<984>	VSS<904>	M79
W26	VSS<983>	VSS<903>	M77
W24	VSS<982>	VSS<902>	M75
W18	VSS<981>	VSS<901>	M73
W12	VSS<980>	VSS<900>	M71
V25	VSS<979>	VSS<899>	M69
U86	VSS<978>	VSS<898>	M67
U80	VSS<977>	VSS<897>	M65
U8	VSS<976>	VSS<896>	M63
U74	VSS<975>	VSS<895>	M61
U68	VSS<974>	VSS<894>	M59
U62	VSS<973>	VSS<893>	M57
U6	VSS<972>	VSS<892>	M55
U56	VSS<971>	VSS<891>	M53
U4	VSS<970>	VSS<890>	M3
U28	VSS<969>	VSS<889>	M27
U24	VSS<968>	VSS<888>	M21
U22	VSS<967>	VSS<887>	M15
U20	VSS<966>	VSS<886>	K9
U2	VSS<965>	VSS<885>	K85
U18	VSS<964>	VSS<884>	K83
U16	VSS<963>	VSS<883>	K77
U14	VSS<962>	VSS<882>	K71
U12	VSS<961>	VSS<881>	K7
U10	VSS<960>	VSS<880>	K65
T85	VSS<959>	VSS<879>	K59
T81	VSS<958>	VSS<878>	K53
T79	VSS<957>	VSS<877>	K5
T75	VSS<956>	VSS<876>	K3
T73	VSS<955>	VSS<875>	K27
T69	VSS<954>	VSS<874>	K25
T67	VSS<953>	VSS<873>	K23
T63	VSS<952>	VSS<872>	K21
T61	VSS<951>	VSS<871>	K19
T57	VSS<950>	VSS<870>	K17
T55	VSS<949>	VSS<869>	K15
T25	VSS<948>	VSS<868>	K13
R84	VSS<947>	VSS<867>	K11
R82	VSS<946>	VSS<866>	J82
R78	VSS<945>	VSS<865>	J78
R76	VSS<944>	VSS<864>	J76
R72	VSS<943>	VSS<863>	J72
R70	VSS<942>	VSS<862>	J70
R66	VSS<941>	VSS<861>	J66
R64	VSS<940>	VSS<860>	J64
R60	VSS<939>	VSS<859>	J60
R6	VSS<938>	VSS<858>	J58
R58	VSS<937>	VSS<857>	J54
R54	VSS<936>	VSS<856>	J2
R28	VSS<935>	VSS<855>	H9
R24	VSS<934>	VSS<854>	H85
R18	VSS<933>	VSS<853>	H83
R12	VSS<932>	VSS<852>	H81
P83	VSS<931>	VSS<851>	H79
P77	VSS<930>	VSS<850>	H75
P71	VSS<929>	VSS<849>	H73
P7	VSS<928>	VSS<848>	H63

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KNL_LGA_SKPP_EXT

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H27	VSS<843>	VSS<761>	DY73
H21	VSS<842>	VSS<760>	DY71
H15	VSS<841>	VSS<759>	DY7
G84	VSS<840>	VSS<758>	DY61
G80	VSS<839>	VSS<757>	DY59
G8	VSS<838>	VSS<756>	DY55
G74	VSS<837>	VSS<755>	DY5
G62	VSS<836>	VSS<754>	DY3
G56	VSS<835>	VSS<753>	DY25
G54	VSS<834>	VSS<752>	DY15
G4	VSS<833>	VSS<751>	DY13
G26	VSS<832>	VSS<750>	DY11
G16	VSS<831>	VSS<749>	DW84
G14	VSS<830>	VSS<748>	DW8
G10	VSS<829>	VSS<747>	DW78
F83	VSS<828>	VSS<746>	DW72
F81	VSS<827>	VSS<745>	DW66
F79	VSS<826>	VSS<744>	DW60
F77	VSS<825>	VSS<743>	DW54
F75	VSS<824>	VSS<742>	DW4
F73	VSS<823>	VSS<741>	DW26
F71	VSS<822>	VSS<740>	DW14
F7	VSS<821>	VSS<739>	DW10
F5	VSS<820>	VSS<738>	DV9
F45	VSS<819>	VSS<737>	DV3
F43	VSS<818>	VSS<736>	DV27
F3	VSS<817>	VSS<735>	DV21
F27	VSS<816>	VSS<734>	DV15
F25	VSS<815>	VSS<733>	DU84
F17	VSS<814>	VSS<732>	DU82
F13	VSS<813>	VSS<731>	DU80
F11	VSS<812>	VSS<730>	DU78
EC84	VSS<811>	VSS<729>	DU76
EC80	VSS<810>	VSS<728>	DU74
EC46	VSS<809>	VSS<727>	DU72
EC40	VSS<808>	VSS<726>	DU70
EB81	VSS<807>	VSS<725>	DU68
EB75	VSS<806>	VSS<724>	DU66
EB71	VSS<805>	VSS<723>	DU64
EB63	VSS<804>	VSS<722>	DU62
EB57	VSS<803>	VSS<721>	DU60
EB55	VSS<802>	VSS<720>	DU58
EB5	VSS<801>	VSS<719>	DU56
EB45	VSS<800>	VSS<718>	DU54
EB41	VSS<799>	VSS<717>	DT9
EB11	VSS<798>	VSS<716>	DT85
EA84	VSS<795>	VSS<715>	DT7
EA82	VSS<794>	VSS<714>	DT5
EA80	VSS<793>	VSS<713>	DT3
EA8	VSS<792>	VSS<712>	DT27
EA76	VSS<791>	VSS<711>	DK25
EA74	VSS<790>	VSS<710>	DK23
EA72	VSS<789>	VSS<709>	DK21
EA70	VSS<788>	VSS<708>	DK19
EA62	VSS<787>	VSS<707>	DK17
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EA42	VSS<782>	VSS<702>	DR78
EA16	VSS<781>	VSS<701>	DR72
EA14	VSS<780>	VSS<700>	DR66
EA12	VSS<779>	VSS<699>	DR60
E82	VSS<778>	VSS<698>	DR54
E80	VSS<777>	VSS<697>	DR2
E78	VSS<776>	VSS<696>	DP9
E76	VSS<775>	VSS<695>	DP83
E74	VSS<774>	VSS<694>	DP79
E72	VSS<773>	VSS<693>	DP77
E6	VSS<772>	VSS<692>	DP73
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E42	VSS<769>	VSS<689>	DP65
E24	VSS<768>	VSS<688>	DP61
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DN82	VSS<681>	VSS<601>	DG56
DN80	VSS<680>	VSS<600>	DG24
DN8	VSS<679>	VSS<599>	DG18
DN76	VSS<678>	VSS<598>	DG12
DN74	VSS<677>	VSS<597>	DF83
DN70	VSS<676>	VSS<596>	DF79
DN68	VSS<675>	VSS<595>	DF77
DN64	VSS<674>	VSS<594>	DF73
DN62	VSS<673>	VSS<593>	DF71
DN58	VSS<672>	VSS<592>	DF7
DN56	VSS<671>	VSS<591>	DF67
DN4	VSS<670>	VSS<590>	DF65
DN26	VSS<669>	VSS<589>	DF61
DN22	VSS<668>	VSS<588>	DF59
DN20	VSS<667>	VSS<587>	DF55
DN16	VSS<666>	VSS<586>	DF5
DN14	VSS<665>	VSS<585>	DF27
DN10	VSS<664>	VSS<584>	DF25
DM81	VSS<663>	VSS<583>	DF23
DM75	VSS<662>	VSS<582>	DF19
DM7	VSS<661>	VSS<581>	DF17
DM69	VSS<660>	VSS<580>	DF13
DM63	VSS<659>	VSS<579>	DF11
DM57	VSS<658>	VSS<578>	DE84
DM5	VSS<657>	VSS<577>	DE8
DM25	VSS<656>	VSS<576>	DE78
DM23	VSS<655>	VSS<575>	DE72
DM19	VSS<654>	VSS<574>	DE66
DM17	VSS<653>	VSS<573>	DE60
DM13	VSS<652>	VSS<572>	DE54
DM11	VSS<651>	VSS<571>	DE42
DL6	VSS<650>	VSS<570>	DE4
DL56	VSS<649>	VSS<569>	DE30
DL24	VSS<648>	VSS<568>	DE26
DL18	VSS<647>	VSS<567>	DE22
DL12	VSS<646>	VSS<566>	DE20
DK85	VSS<645>	VSS<565>	DE16
DK83	VSS<644>	VSS<564>	DE14
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DK77	VSS<641>	VSS<561>	DO85
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DK71	VSS<638>	VSS<558>	DO33
DK69	VSS<637>	VSS<557>	DO31
DK67	VSS<636>	VSS<556>	DO3
DK65	VSS<635>	VSS<555>	DO29
DK63	VSS<634>	VSS<554>	DO27
DK61	VSS<633>	VSS<553>	DO21
DK59	VSS<632>	VSS<552>	DO15
DK57	VSS<631>	VSS<551>	DC84
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DJ56	VSS<628>	VSS<548>	DC78
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DJ4	VSS<626>	VSS<546>	DC74
DJ24	VSS<625>	VSS<545>	DC72
DJ22	VSS<624>	VSS<544>	DC70
DJ20	VSS<623>	VSS<543>	DC68
DJ2	VSS<622>	VSS<542>	DC66
DJ18	VSS<621>	VSS<541>	DC64
DJ16	VSS<620>	VSS<540>	DC62
DJ14	VSS<619>	VSS<539>	DC60
DJ12	VSS<618>	VSS<538>	DC58
DJ10	VSS<617>	VSS<537>	DC56
DH81	VSS<616>	VSS<536>	DC54
DH75	VSS<615>	VSS<535>	DC50
DH69	VSS<614>	VSS<534>	DC48
DH63	VSS<613>	VSS<533>	DC46
DH57	VSS<612>	VSS<532>	DC44
DG82	VSS<611>	VSS<531>	DC42
DG80	VSS<610>	VSS<530>	DC40
DG76	VSS<609>	VSS<529>	DC38
DG74	VSS<608>	VSS<528>	DC36
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DB37	VSS<519>	VSS<439>	CV63
DB35	VSS<518>	VSS<438>	CV61
DB3	VSS<517>	VSS<437>	CV57
DB27	VSS<516>	VSS<436>	CV5
DB25	VSS<515>	VSS<435>	CV25
DB23	VSS<514>	VSS<434>	CV23
DB21	VSS<513>	VSS<433>	CV19
DB19	VSS<512>	VSS<432>	CV17
DB17	VSS<511>	VSS<431>	CV13
DB15	VSS<510>	VSS<430>	CV11
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DB11	VSS<508>	VSS<428>	CU80
DA84	VSS<507>	VSS<427>	CU8
DA78	VSS<506>	VSS<426>	CU78
DA72	VSS<505>	VSS<425>	CU76
DA66	VSS<504>	VSS<424>	CU60
DA60	VSS<503>	VSS<423>	CU6
DA54	VSS<502>	VSS<422>	CU56
DA50	VSS<501>	VSS<421>	CU32
DA44	VSS<500>	VSS<420>	CU28
DA42	VSS<499>	VSS<419>	CU26
DA34	VSS<498>	VSS<418>	CU24
D47	VSS<497>	VSS<417>	CU18
D41	VSS<496>	VSS<416>	CU14
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CY85	VSS<494>	VSS<414>	CU10
CY83	VSS<493>	VSS<413>	CT7
CY79	VSS<492>	VSS<412>	CT67
CY77	VSS<491>	VSS<411>	CT65
CY73	VSS<490>	VSS<410>	CT55
CY71	VSS<489>	VSS<409>	CT31
CY67	VSS<488>	VSS<408>	CT19
CY65	VSS<487>	VSS<407>	CR80
CY61	VSS<486>	VSS<406>	CR8
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CY41	VSS<480>	VSS<400>	CP83
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CY37	VSS<478>	VSS<398>	CP67
CY35	VSS<477>	VSS<397>	CP65
CY33	VSS<476>	VSS<396>	CP61
CY3	VSS<475>	VSS<395>	CP55
CY27	VSS<474>	VSS<394>	CP23
CY21	VSS<473>	VSS<393>	CP19
CY15	VSS<472>	VSS<392>	CN86
CW86	VSS<471>	VSS<391>	CN84
CW82	VSS<470>	VSS<390>	CN82
CW80	VSS<469>	VSS<389>	CN80
CW8	VSS<468>	VSS<388>	CN8
CW76	VSS<467>	VSS<387>	CN78
CW74	VSS<466>	VSS<386>	CN76
CW68	VSS<465>	VSS<385>	CN74
CW64	VSS<464>	VSS<384>	CN70
CW62	VSS<463>	VSS<383>	CN62
CW58	VSS<462>	VSS<382>	CN6
CW56	VSS<461>	VSS<381>	CN22
CW50	VSS<460>	VSS<380>	CN20
CW48	VSS<459>	VSS<379>	CN2
CW46	VSS<458>	VSS<378>	CN10
CW4	VSS<457>	VSS<377>	CN85
CW32	VSS<456>	VSS<376>	CM83
CW30	VSS<455>	VSS<375>	CM81
CW28	VSS<454>	VSS<374>	CM79
CW26	VSS<453>	VSS<373>	CM77
CW22	VSS<452>	VSS<372>	CM75
CW20	VSS<451>	VSS<371>	CM73
CW2	VSS<450>	VSS<370>	CM71
CW16	VSS<449>	VSS<369>	CM7
CW14	VSS<448>	VSS<368>	CM69
CW10	VSS<447>	VSS<367>	CM65
CV9	VSS<446>	VSS<366>	CM5

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CM11	VSS<362>	VSS<282>	CC22
CM1	VSS<361>	VSS<281>	CC20
CL68	VSS<360>	VSS<280>	CC2
CL26	VSS<359>	VSS<279>	CC18
CL16	VSS<358>	VSS<278>	CC16
CL12	VSS<357>	VSS<277>	CC14
CL10	VSS<356>	VSS<276>	CC12
CK85	VSS<355>	VSS<275>	CC10
CK65	VSS<354>	VSS<274>	CB67
CK63	VSS<353>	VSS<273>	CA84
CK61	VSS<352>	VSS<272>	CA82
CK59	VSS<351>	VSS<271>	CA80
CK25	VSS<350>	VSS<270>	CA78
CK19	VSS<349>	VSS<269>	CA76
CK15	VSS<348>	VSS<268>	CA74
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CJ60	VSS<346>	VSS<266>	CA70
CJ24	VSS<345>	VSS<265>	CA68
CJ22	VSS<344>	VSS<264>	BY83
CJ18	VSS<343>	VSS<263>	BY18
CJ14	VSS<342>	VSS<262>	BY79
CJ12	VSS<341>	VSS<261>	BY77
CH9	VSS<340>	VSS<260>	BY75
CH85	VSS<339>	VSS<259>	BY73
CH7	VSS<338>	VSS<258>	BY71
CH65	VSS<337>	VSS<257>	BY69
CH25	VSS<336>	VSS<256>	BY65
CH23	VSS<335>	VSS<255>	BY63
CH21	VSS<334>	VSS<254>	BW68
CH19	VSS<333>	VSS<253>	BU8
CH17	VSS<332>	VSS<252>	BU68
CH15	VSS<331>	VSS<251>	BU64
CH11	VSS<330>	VSS<250>	BU60
CG84	VSS<329>	VSS<249>	BU6
CG82	VSS<328>	VSS<248>	BU4
CG80	VSS<327>	VSS<247>	BU26
CG78	VSS<326>	VSS<246>	BU24
CG76	VSS<325>	VSS<245>	BU22
CG74	VSS<324>	VSS<244>	BU20
CG72	VSS<323>	VSS<243>	BU18
CG70	VSS<322>	VSS<242>	BU16
CG68	VSS<321>	VSS<241>	BU14
CF85	VSS<320>	VSS<240>	BU12
CF83	VSS<319>	VSS<239>	BU10
CF81	VSS<318>	VSS<238>	BT9
CF79	VSS<317>	VSS<237>	BT7
CF77	VSS<316>	VSS<236>	BT63
CF75	VSS<315>	VSS<235>	BT5
CF73	VSS<314>	VSS<234>	BT27
CF71	VSS<313>	VSS<233>	BT25
CF69	VSS<312>	VSS<232>	BT23
CF65	VSS<311>	VSS<231>	BT21
CF25	VSS<310>	VSS<230>	BT19
CF19	VSS<309>	VSS<229>	BT17
CE68	VSS<308>	VSS<228>	BT15
CE62	VSS<307>	VSS<227>	BT13
CD9	VSS<306>	VSS<226>	BT11
CD85	VSS<305>	VSS<225>	BR84
CD7	VSS<304>	VSS<224>	BR82
CD67	VSS<303>	VSS<223>	BR80
CD65	VSS<302>	VSS<222>	BR78
CD5	VSS<301>	VSS<221>	BR76
CD3	VSS<300>	VSS<220>	BR74
CD27	VSS<299>	VSS<219>	BR72
CD25	VSS<298>	VSS<218>	BR70
CD23	VSS<297>	VSS<217>	BR68
CD21	VSS<296>	VSS<216>	BP83
CD19	VSS<295>	VSS<215>	BP81
CD17	VSS<294>	VSS<214>	BP79
CD15	VSS<293>	VSS<213>	BP77
CD13	VSS<292>	VSS<212>	BP75
CD11	VSS<291>	VSS<211>	BP73
CC8	VSS<290>	VSS<210>	BP71
CC68	VSS<289>	VSS<209>	BP69
CC64	VSS<288>	VSS<208>	BP67
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CC6	VSS<286>	VSS<206>	BM67

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BL60	VSS<201>	VSS<121>	BC74
BL6	VSS<200>	VSS<120>	BC72
BL4	VSS<199>	VSS<119>	BC68
BL26	VSS<198>	VSS<118>	BC64
BL24	VSS<197>	VSS<117>	BB85
BL22	VSS<196>	VSS<116>	BB83
BL20	VSS<195>	VSS<115>	BB69
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BL16	VSS<193>	VSS<113>	AU74
BL14	VSS<192>	VSS<112>	AU16
BL12	VSS<191>	VSS<111>	AT65
BL10	VSS<190>	VSS<110>	AT11
BK9	VSS<189>	VSS<109>	AP23
BK7	VSS<188>	VSS<108>	AN2
BK67	VSS<187>	VSS<107>	AL68
BK5	VSS<186>	VSS<106>	AK73
BK27	VSS<185>	VSS<105>	AJ76
BK25	VSS<184>	VSS<104>	AJ24
BK23	VSS<183>	VSS<103>	AH53
BK21	VSS<182>	VSS<102>	AG52
BK19	VSS<181>	VSS<101>	AF83
BK17	VSS<180>	VSS<100>	AF61
BK15	VSS<179>	VSS<99>	AF59
BK13	VSS<178>	VSS<98>	AF57
BK11	VSS<177>	VSS<97>	AF55
BJ82	VSS<176>	VSS<96>	AF53
BJ80	VSS<175>	VSS<95>	AF43
BJ78	VSS<174>	VSS<94>	AF41
BJ76	VSS<173>	VSS<93>	AF39
BJ74	VSS<172>	VSS<92>	AF37
BJ72	VSS<171>	VSS<91>	AF35
BJ70	VSS<170>	VSS<90>	AF33
BJ68	VSS<169>	VSS<89>	AF31
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BH81	VSS<167>	VSS<87>	AF29
BH79	VSS<166>	VSS<86>	AF27
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BH71	VSS<162>	VSS<82>	AE34
BH65	VSS<161>	VSS<81>	AE30
BG76	VSS<160>	VSS<80>	AE28
BF77	VSS<159>	VSS<79>	AD9
BF63	VSS<158>	VSS<78>	AD83
BE8	VSS<157>	VSS<77>	AD77
BE76	VSS<156>	VSS<76>	AD71
BE70	VSS<155>	VSS<75>	AD7
BE64	VSS<154>	VSS<74>	AD65
BE60	VSS<153>	VSS<73>	AD59
BE6	VSS<152>	VSS<72>	AD53
BE4	VSS<151>	VSS<71>	AD51
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BE18	VSS<146>	VSS<66>	AD37
BE16	VSS<145>	VSS<65>	AD35
BE14	VSS<144>	VSS<64>	AD3
BE12	VSS<143>	VSS<63>	AD29
BE10	VSS<142>	VSS<62>	AD27
BD9	VSS<141>	VSS<61>	AD25
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BD7	VSS<138>	VSS<58>	AD19
BD5	VSS<137>	VSS<57>	AD17
BD3	VSS<136>	VSS<56>	AD15
BD27	VSS<135>	VSS<55>	AD13
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BD23	VSS<133>	VSS<53>	AC84
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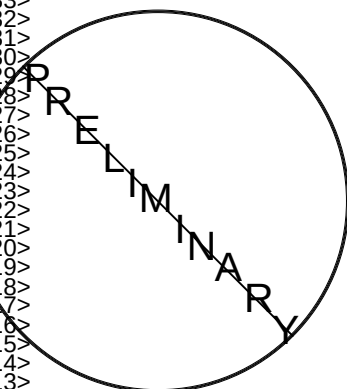
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G7B0B1-001

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KNL_LGA_SKPP_EXT

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	BG66
	BF67
	BF65
	BD67
	BB67
	AY67
	AY65
	AW66



U1
EMPTY

KNL_LGA_SKPP_EXT

NC_CPU_RSVD_1	EF83
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NC_CPU_RSVD_3	EF79
NC_CPU_RSVD_4	EF77
NC_CPU_RSVD_5	EF75
NC_CPU_RSVD_6	EF73
NC_CPU_RSVD_7	EF71
NC_CPU_RSVD_8	EF63
NC_CPU_RSVD_9	EF61
NC_CPU_RSVD_10	EF59
NC_CPU_RSVD_11	EF57
NC_CPU_RSVD_12	EF55
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NC_CPU_RSVD_15	EF49
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DY19	NC_CPU_RSVD_110

U1
EMPTY

KNL_LGA_SKPP_EXT

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C24	NC_CPU_RSVD_202
C18	NC_CPU_RSVD_203
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C14	NC_CPU_RSVD_205
C12	NC_CPU_RSVD_206
C10	NC_CPU_RSVD_207
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C6	NC_CPU_RSVD_209
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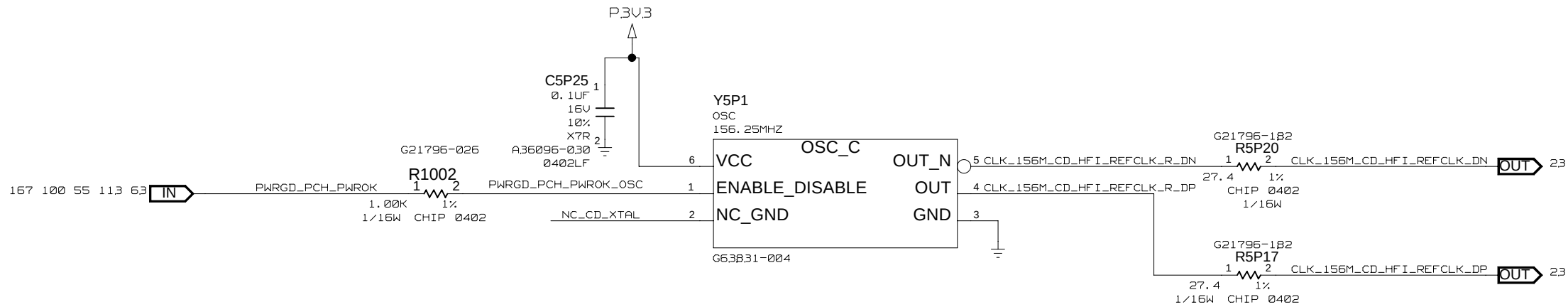
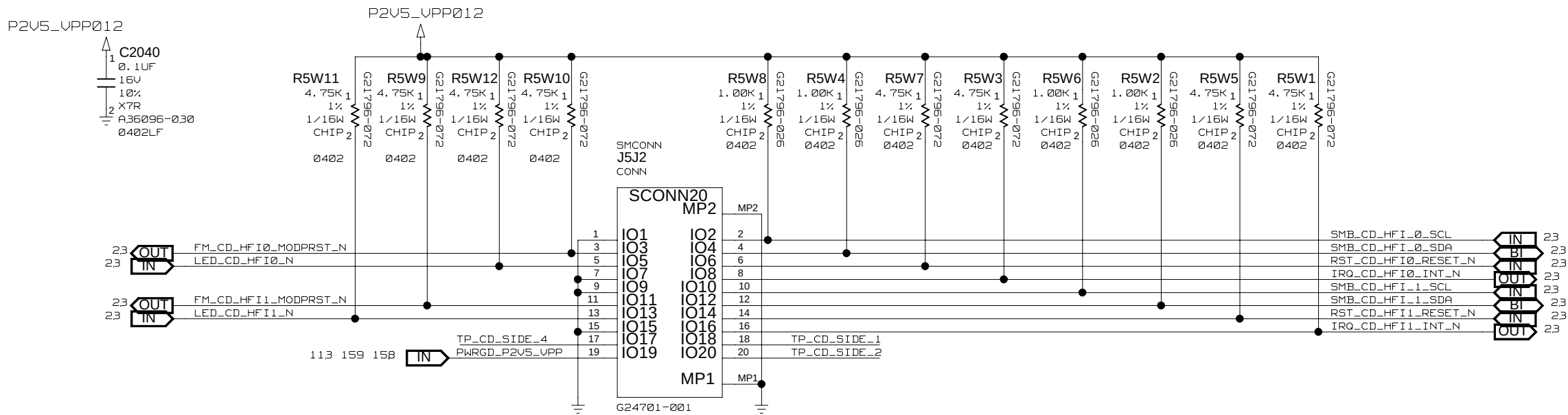
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ROOM: KNL

KNL LGA SPARES

Thu Nov 17 15:19:18 2016

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		SCALE:	DO NOT SCALE DRAWING		SHEET 30 OF 167



INTEL CONFIDENTIAL

CAD NOTE:

PLACE RESISTORS AT SOCKET
OR AS CLOSE AS POSSIBLE

CAD NOTE:

ROUTE ALL VSENSE LINES AS DIFF PAIR
3.5MIL WIDTH, 4MIL SPACING
20MIL AWAY FROM OTHER SIGNALS
TOTAL TRACE RESISTANCE NOT TO EXCEED 1 OHM

CAD NOTE:

PLACE RESISTORS AT SOCKET
OR AS CLOSE AS POSSIBLE

B

B

A

A

ROOM: KNL

Thu Nov 17 15:19:19 2016

KNL SENSE RESISTORS

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
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DDR4 DIMM 0 PAGE 1

ROOM: DDR4_DIMM_0

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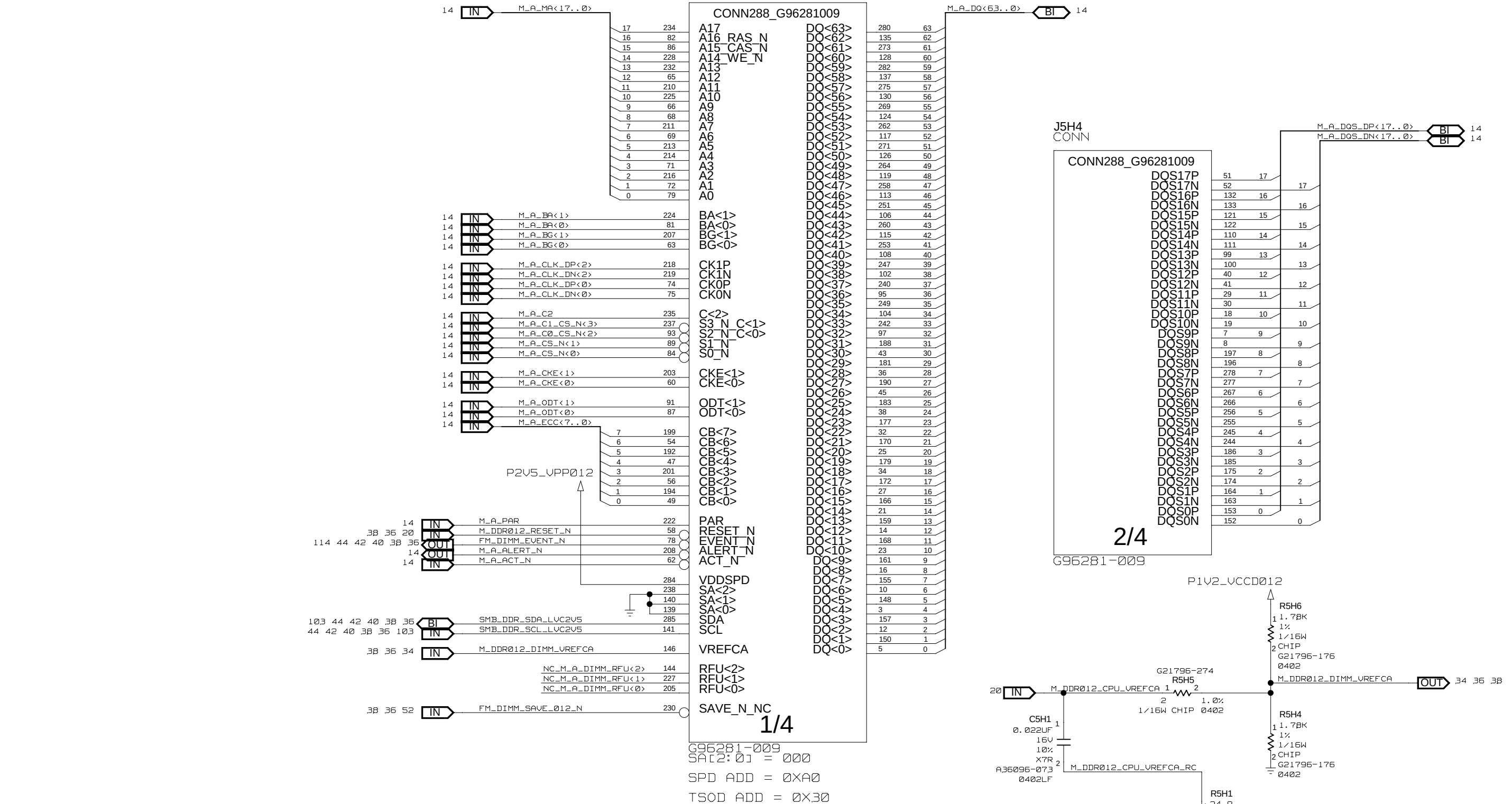
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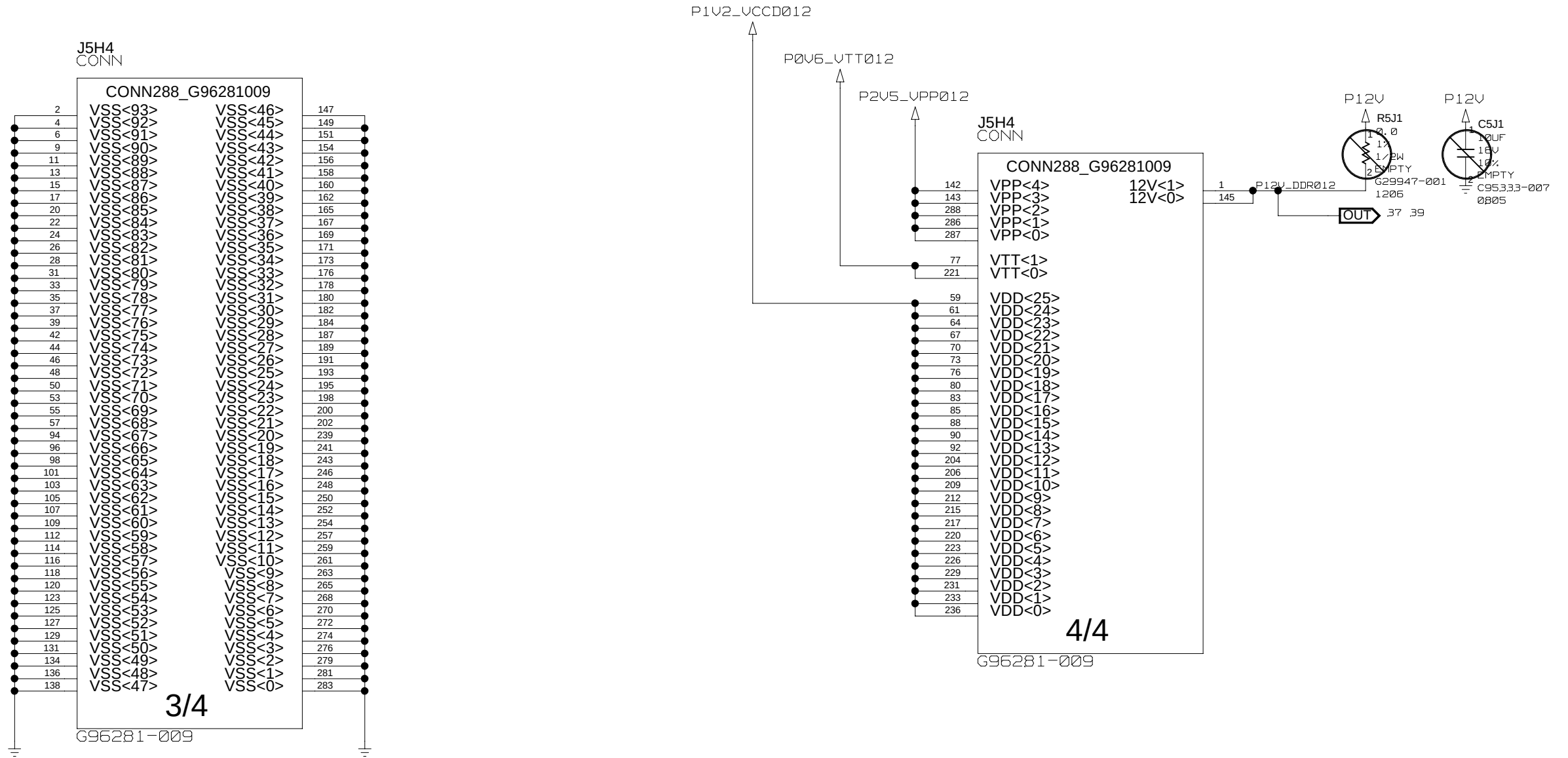
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SHEET 34 OF 167



Thu Nov 17 15:19:19 2016

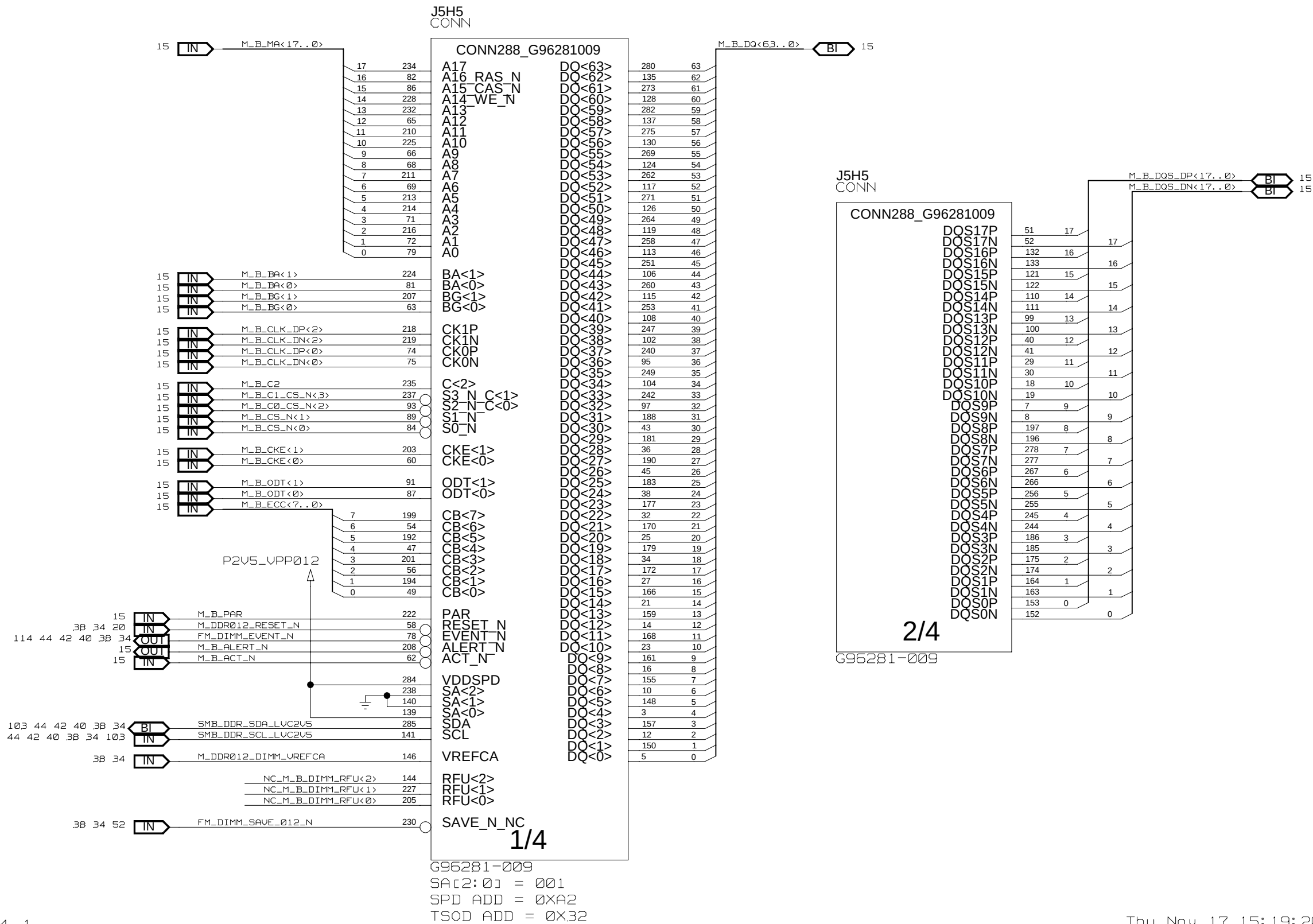


ROOM: DDR4_DIMM_0

DDR4 DIMM 0 PAGE 2

Thu Nov 17 15:19:19 2016

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ROOM: DDR4_DIMM_1

DEPARTMENT

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CODE

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DOCUMENT NUMBER

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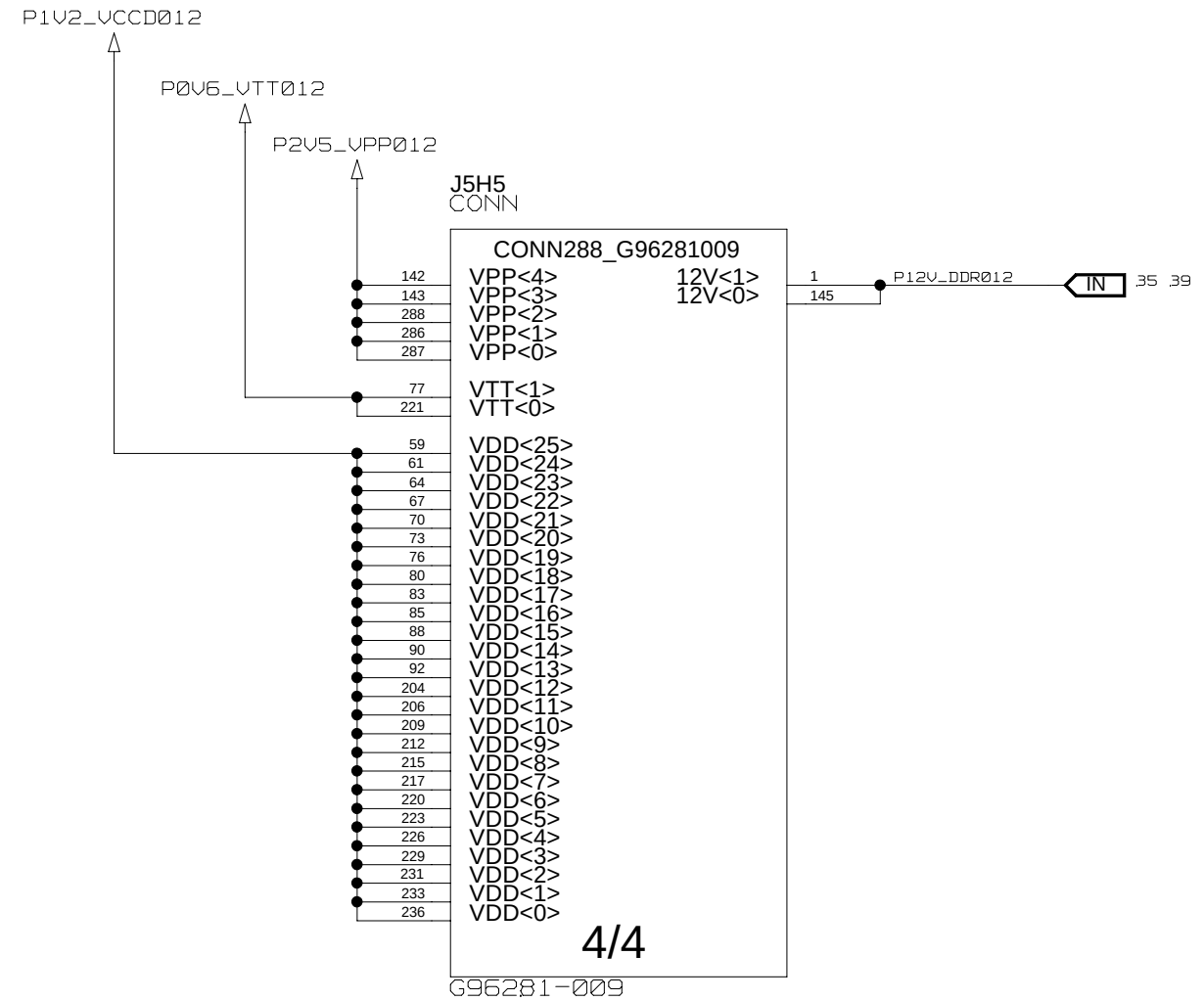
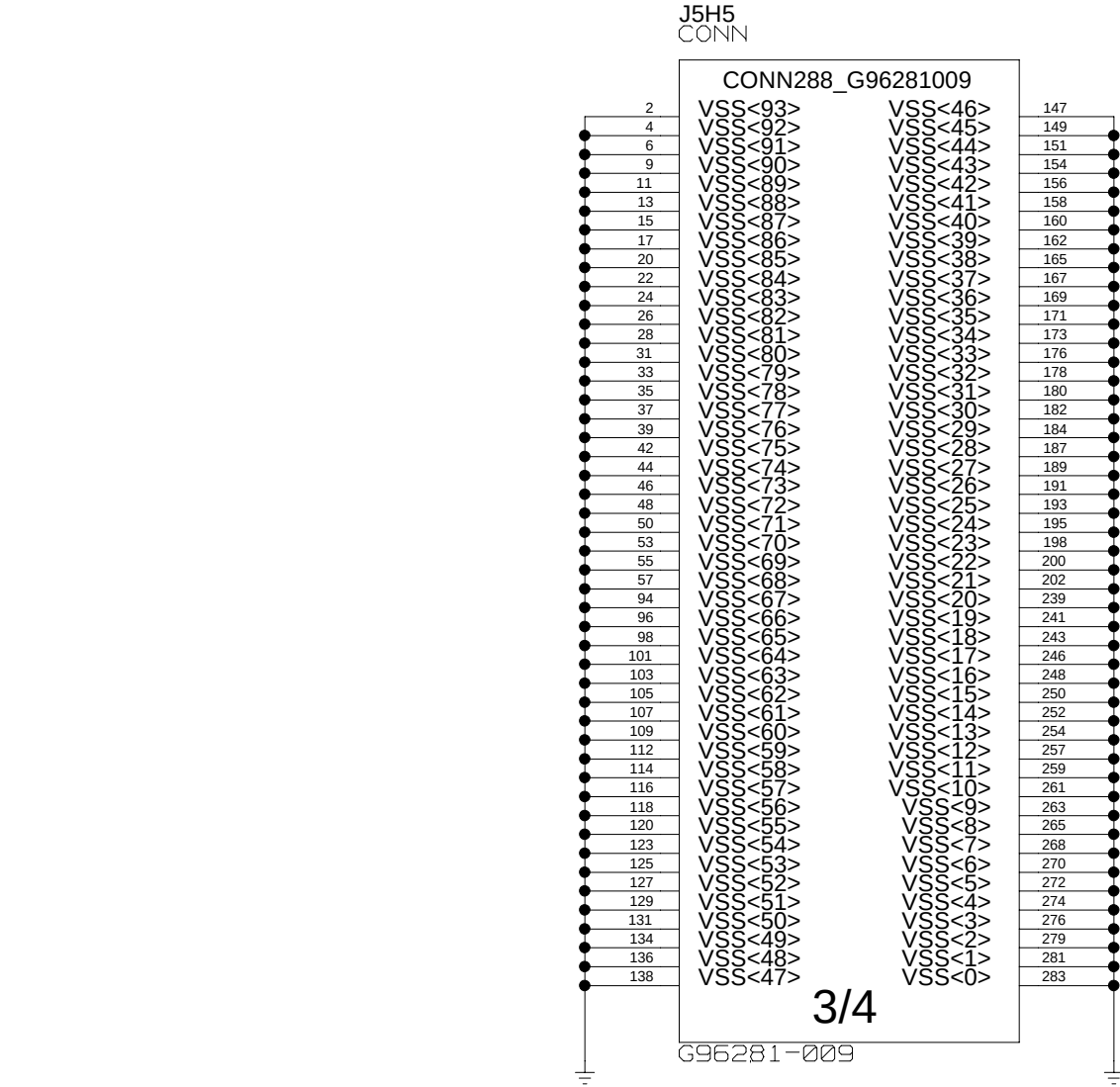
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SHEET 36 OF 167

Thu Nov 17 15:19:20 2016



ROOM: DDR4_DIMM_1

DDR4 DIMM 1 PAGE 2

Thu Nov 17 15:19:20 2016

DEPARTMENT

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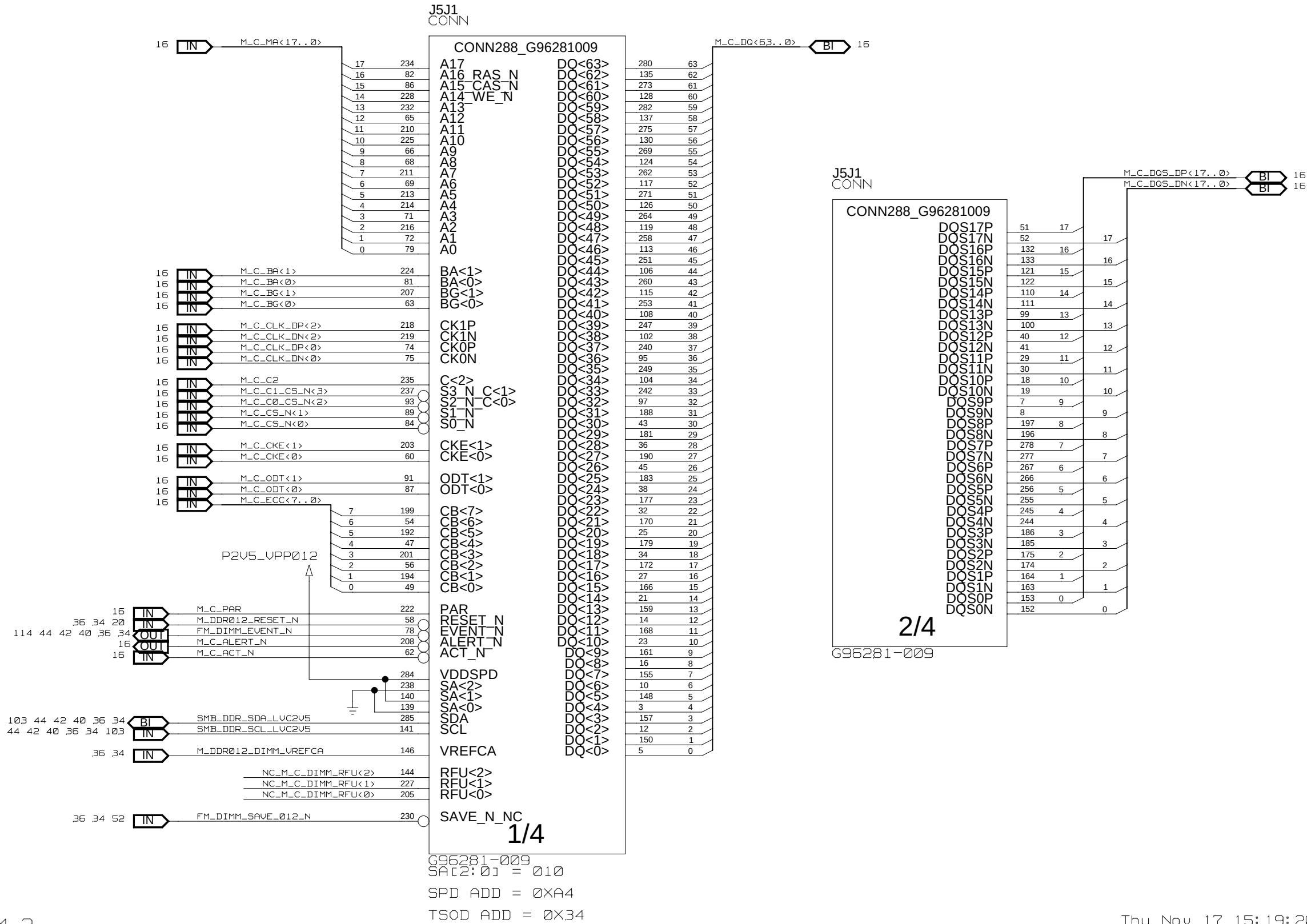
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SHEET .37 OF 167



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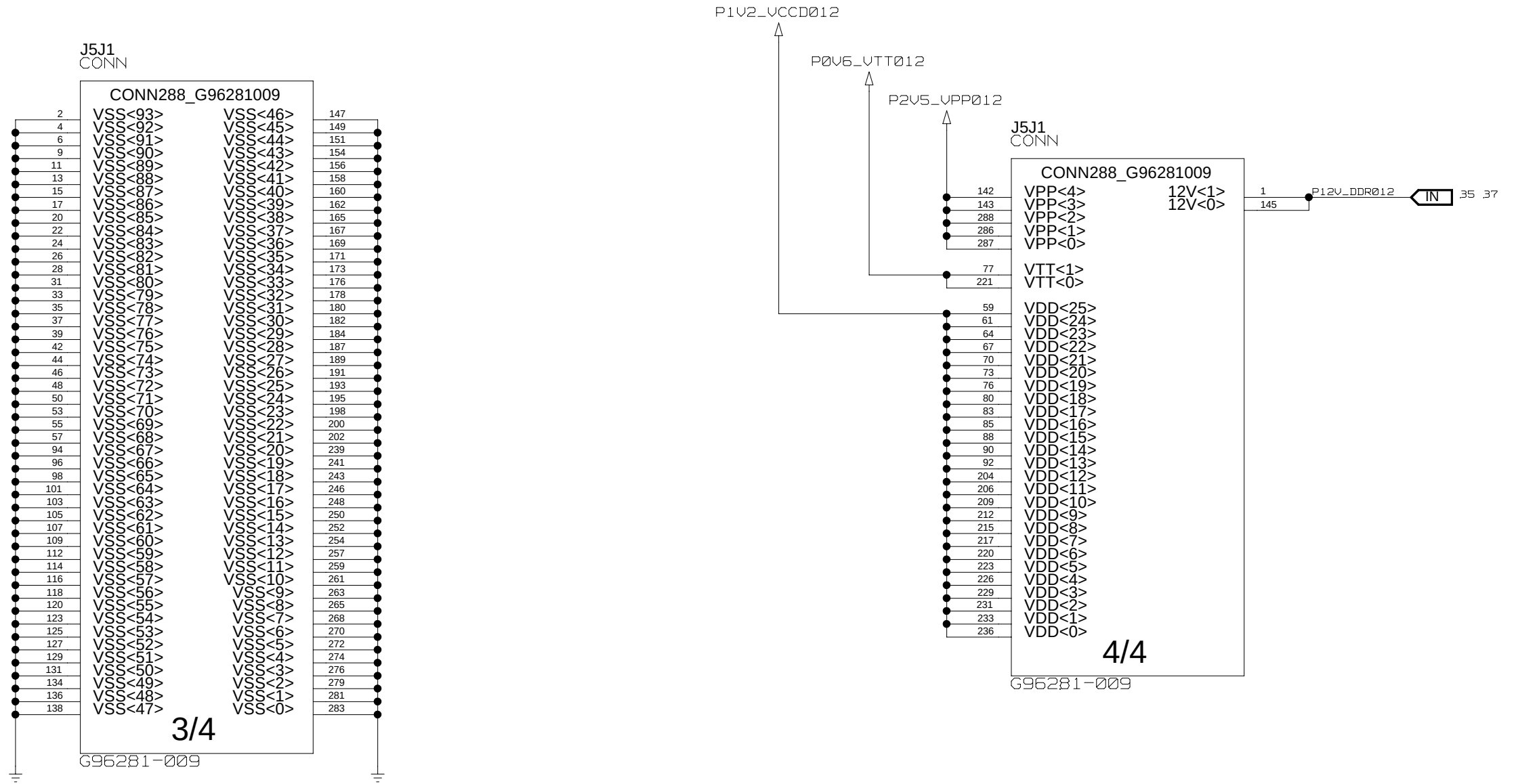
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Santa Clara, CA 95052-8119

SIZE B	CODE 34649	DOCUMENT NUMBER G9428608	REV .3.1.3
SCALE:		DO NOT SCALE DRAWING	SHEET 38 OF 167

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ROOM: DDR4_DIMM_2

DDR4 DIMM 2 PAGE 2

Thu Nov 17 15:19:20 2016

DEPARTMENT

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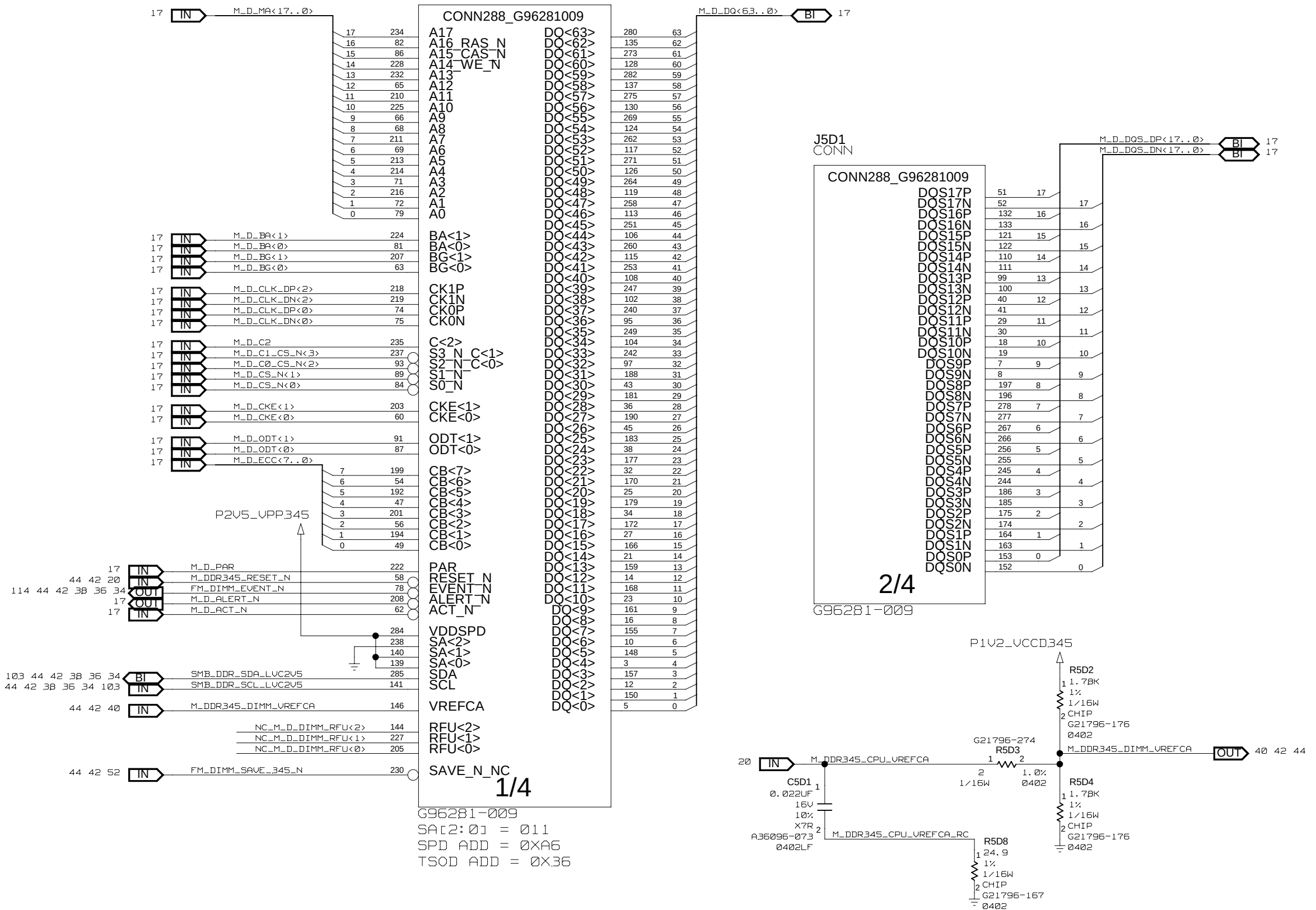
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SHEET 39 OF 167

J5D1
CONN

Thu Nov 17 15:19:21 2016

DEPARTMENT
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Santa Clara, CA 95052-8119

SIZE
B

CODE
34649

DOCUMENT NUMBER
G9428608

REV
3. 1.3

SCALE:

DO NOT SCALE DRAWING

SHEET 40 OF 167



ROOM: DDR4_DIMM_3

DDR4 DIMM 3 PAGE 2

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DEPARTMENT

CBED

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Santa Clara, CA 95052-8119

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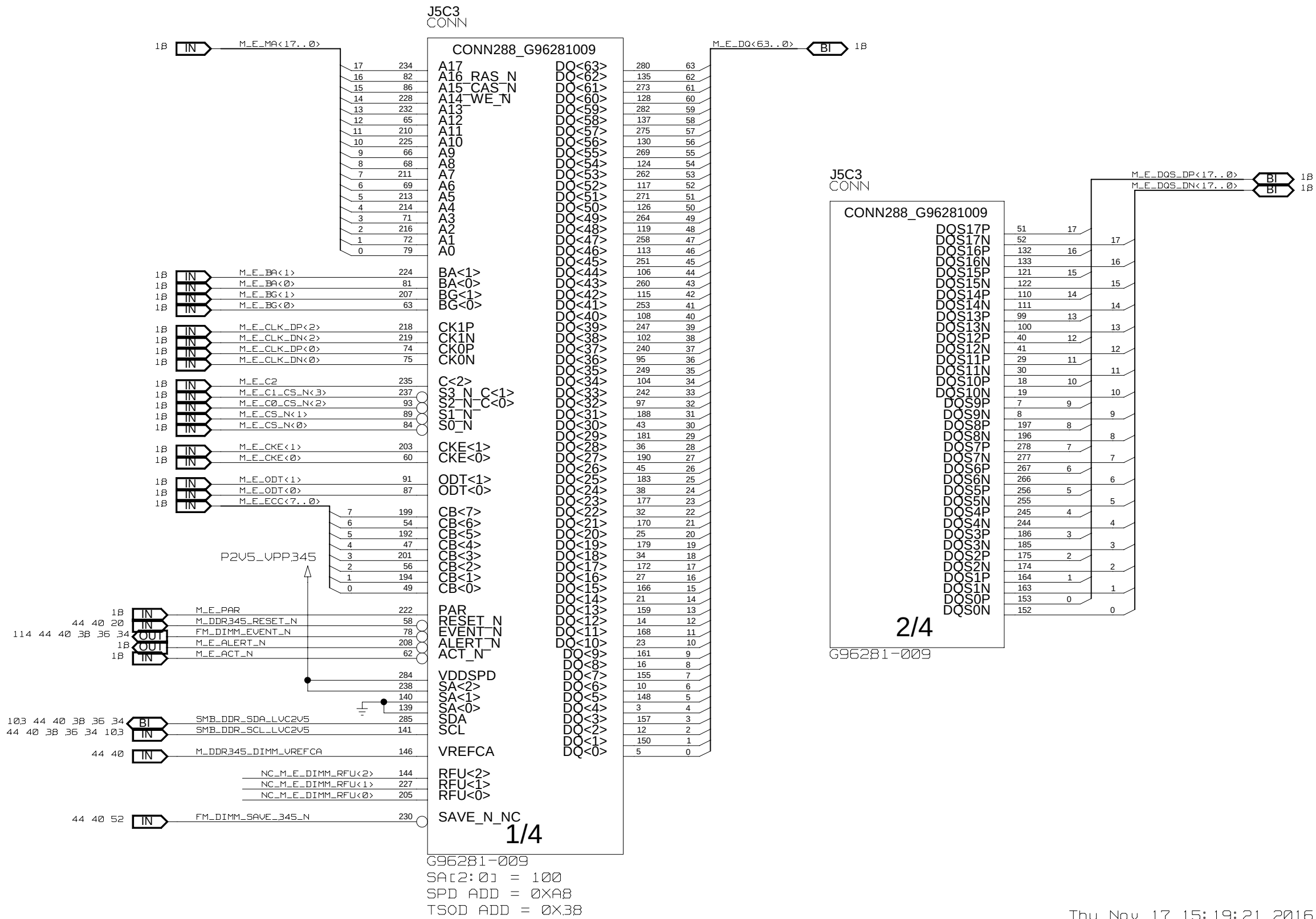
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DO NOT SCALE DRAWING

SHEET 41 OF 167

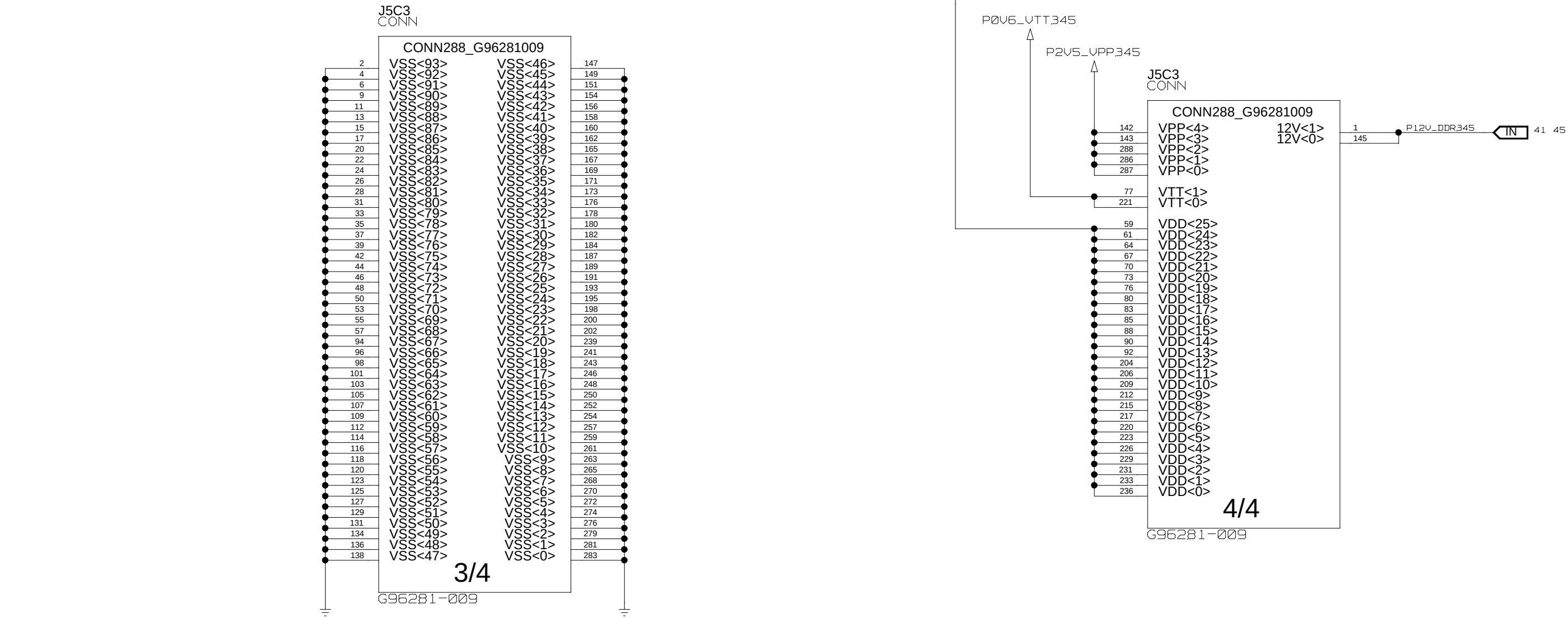


ROOM: DDR4_DIMM_4

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B	34649	G9428608	.3.13
SCALE:	DO NOT SCALE DRAWING		SHEET 42 OF 167

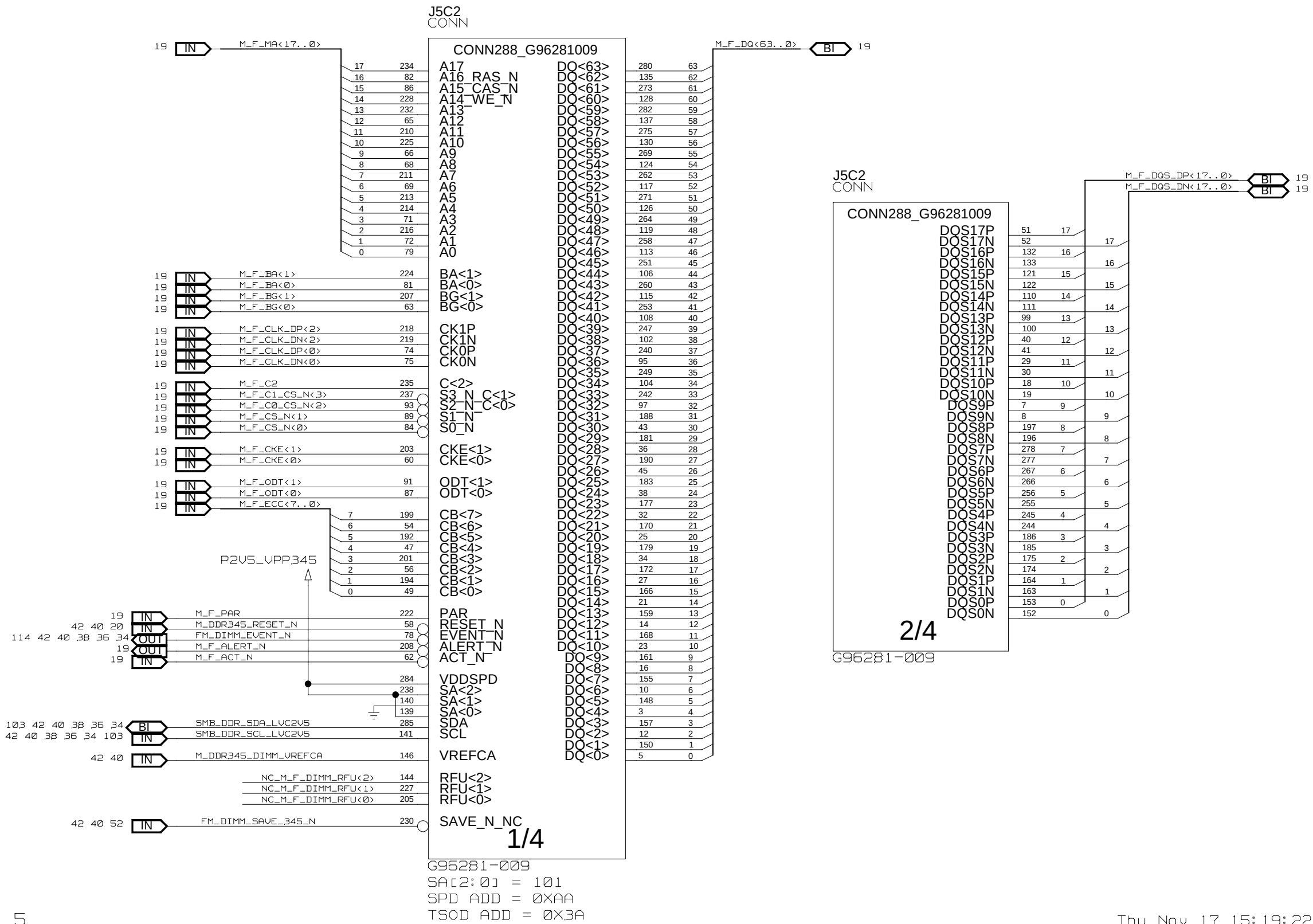


ROOM: DDR4_DIMM_4

DDR4 DIMM 4 PAGE 2

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SCALE:		DO NOT SCALE DRAWING			SHEET 43 OF 167



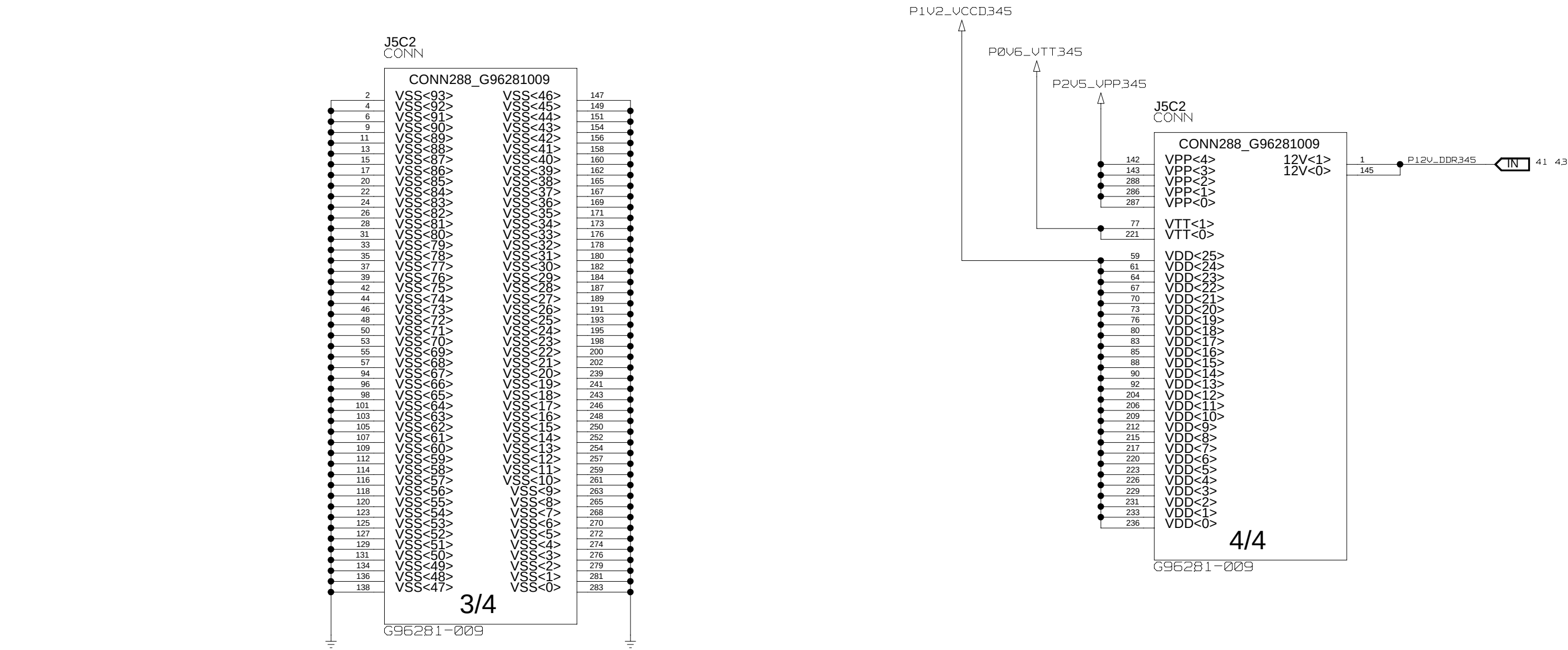
ROOM: DDR4_DIMM_5

DDR4 DIMM 5 PAGE 1

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SCALE:		DO NOT SCALE DRAWING	SHEET 44 OF 167



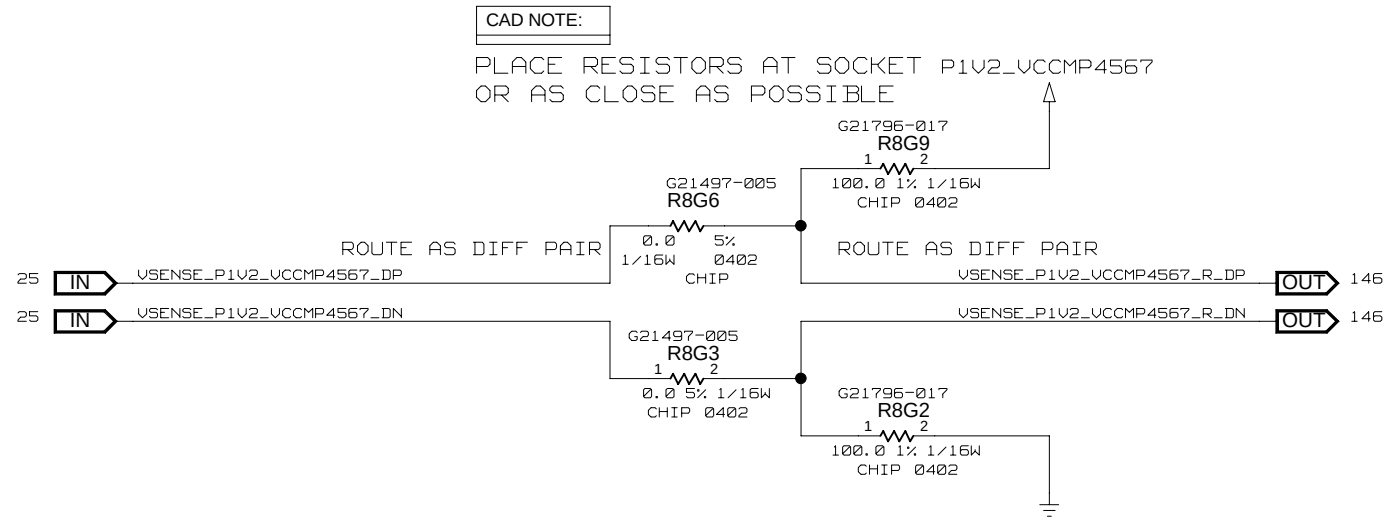
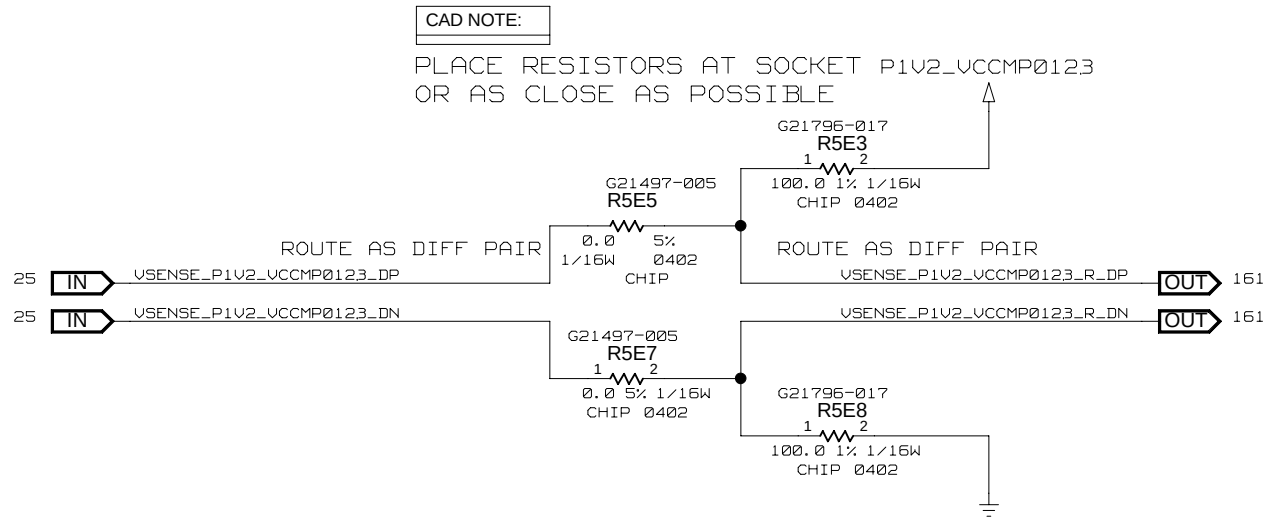
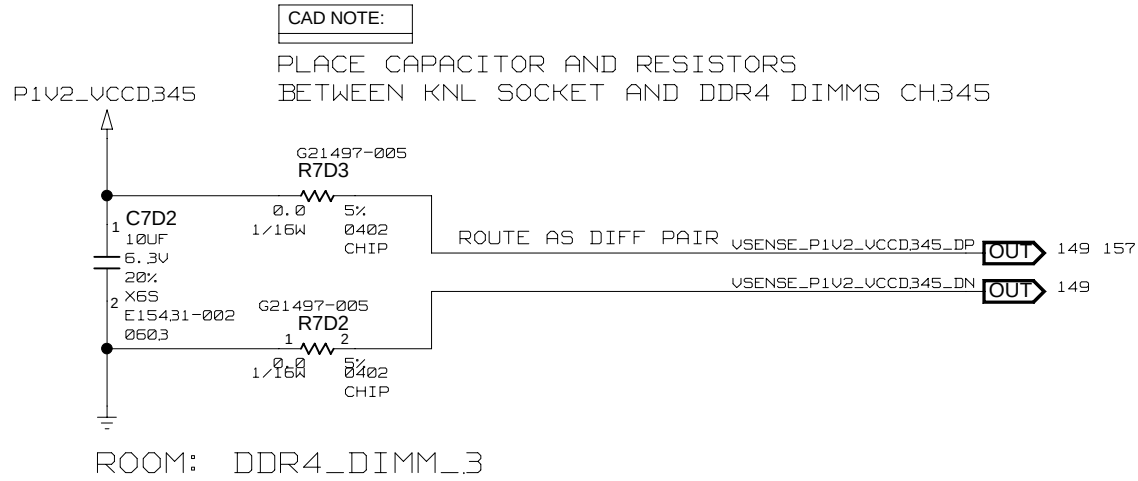
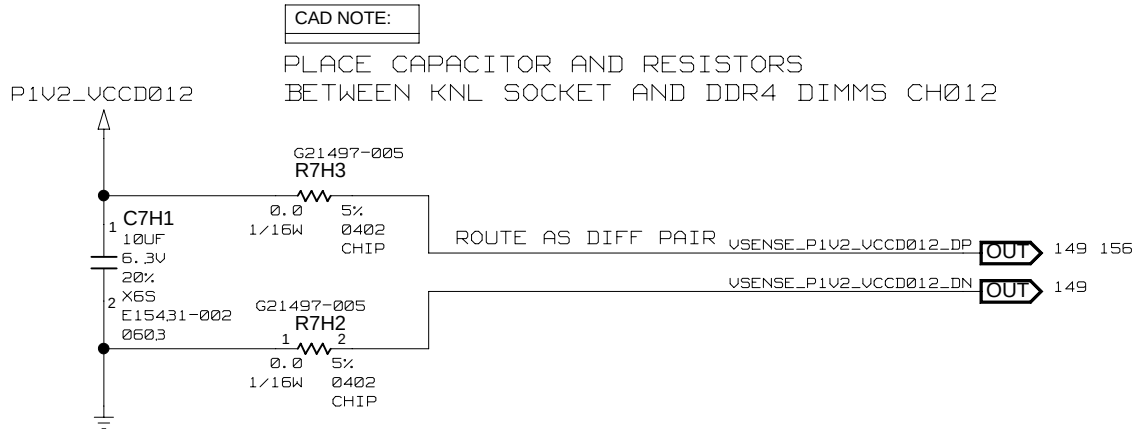
ROOM: DDR4_DIMM_5

DDR4 DIMM 5 PAGE 2

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
CBED	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	G9428608	.3.1.3
SCALE:		DO NOT SCALE DRAWING			SHEET 45 OF 167

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CAD NOTE:
ROUTE ALL VSENSE LINES AS DIFF PAIR
3.5MIL WIDTH, 4MIL SPACING
20MIL AWAY FROM OTHER SIGNALS
TOTAL TRACE RESISTANCE NOT TO EXCEED 1 OHM

ROOM: KNL

VCCD SENSE RESISTORS

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ID	PORT	WIDTH
0	2X8	
1	X16	

ROOM: PCIE_X16_RISER

PCIE X16 SLOT

4

3

2

1

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SCALE:

DO NOT SCALE DRAWING

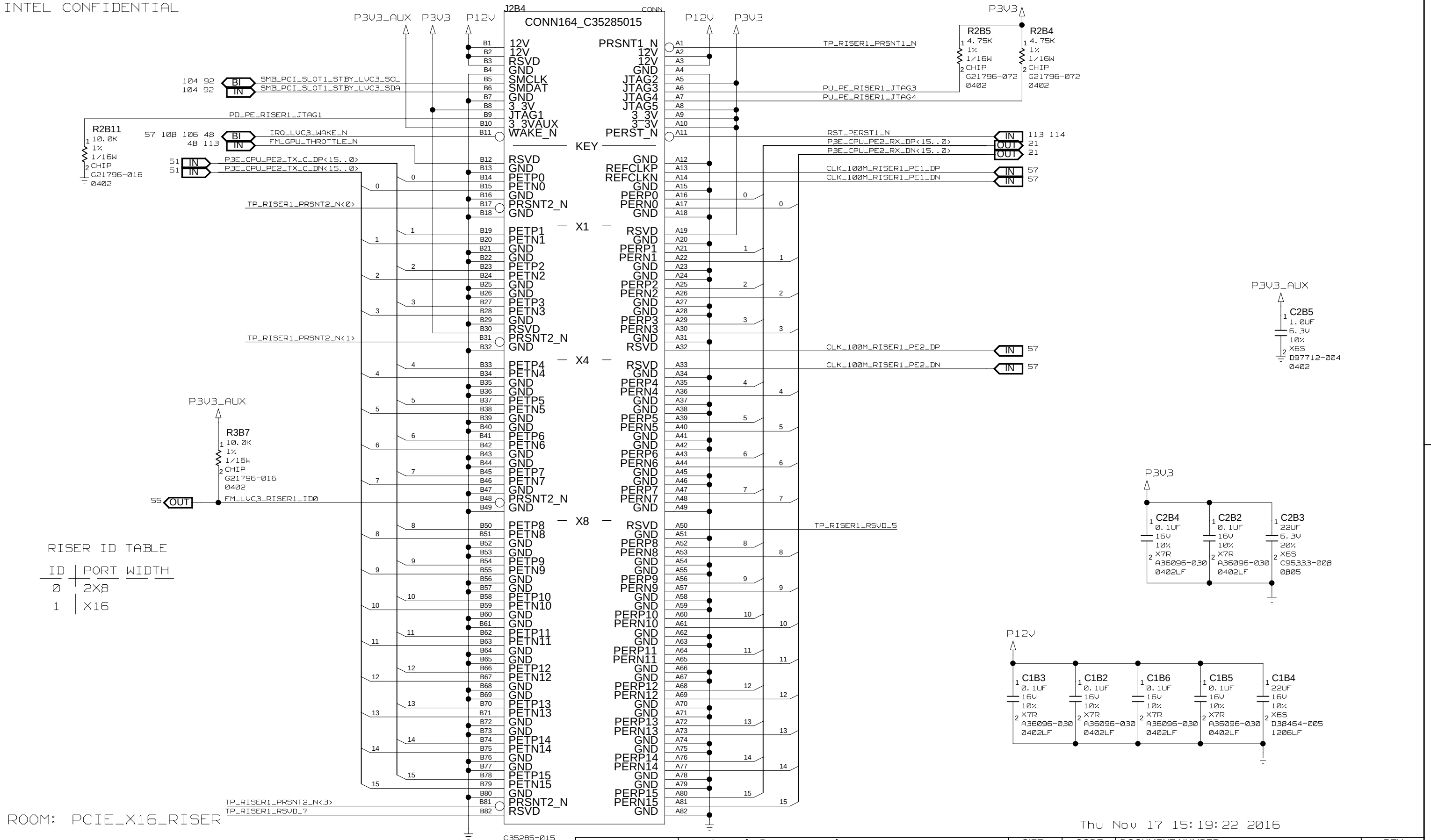
SHEET 47 OF 167

4

3

2

1

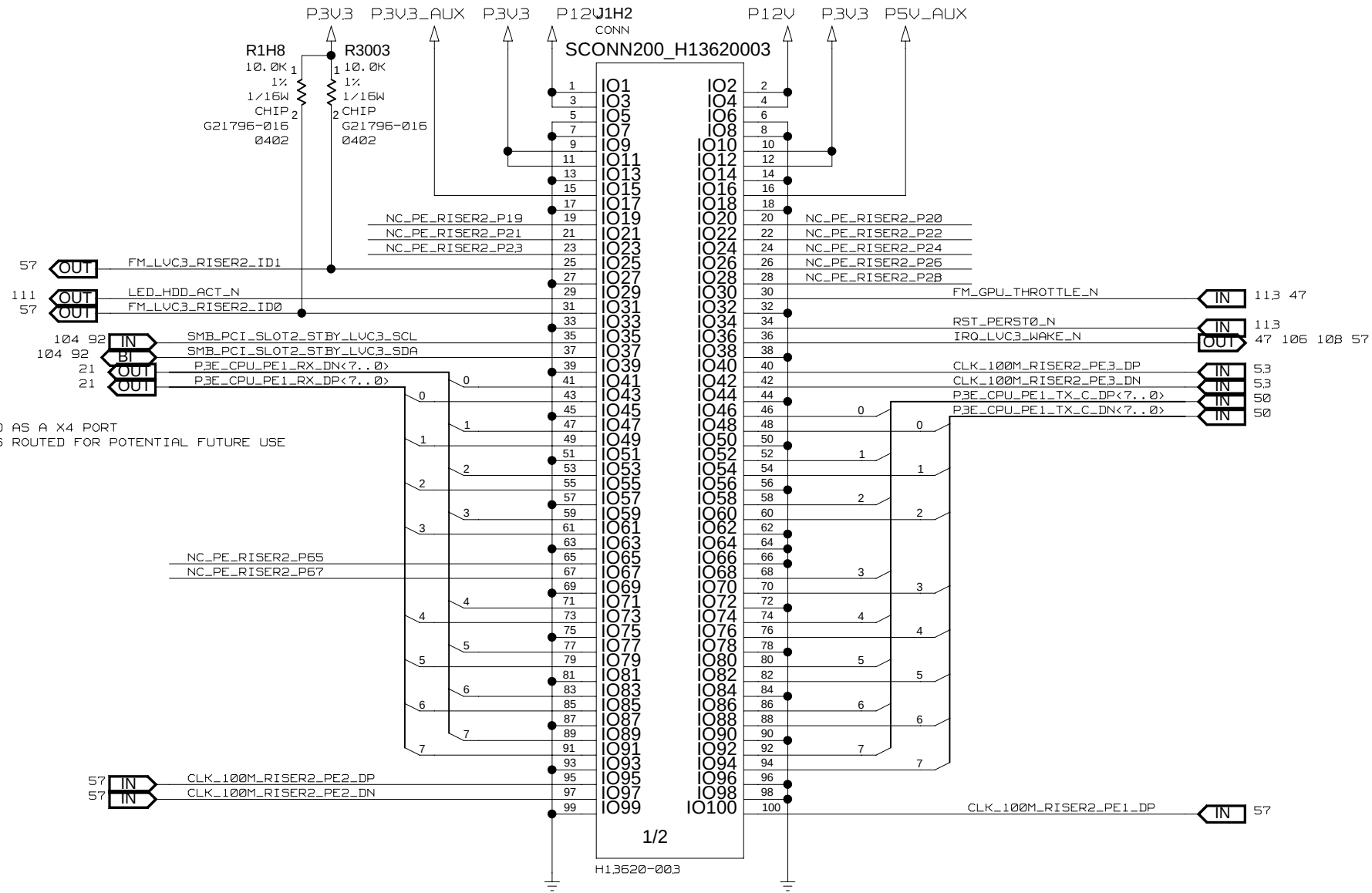


RISER ID TABLE

ID	PORT WIDTH
10	2X8 + X8(OR X4)
11	X16 + X8(OR X4)

DESIGN NOTE:

THIS PORT IS HARD-CODED AS A X4 PORT
THE X8 CONFIGURATION IS ROUTED FOR POTENTIAL FUTURE USE



ROOM: PCIE_X24_RISER

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DOCUMENT NUMBER

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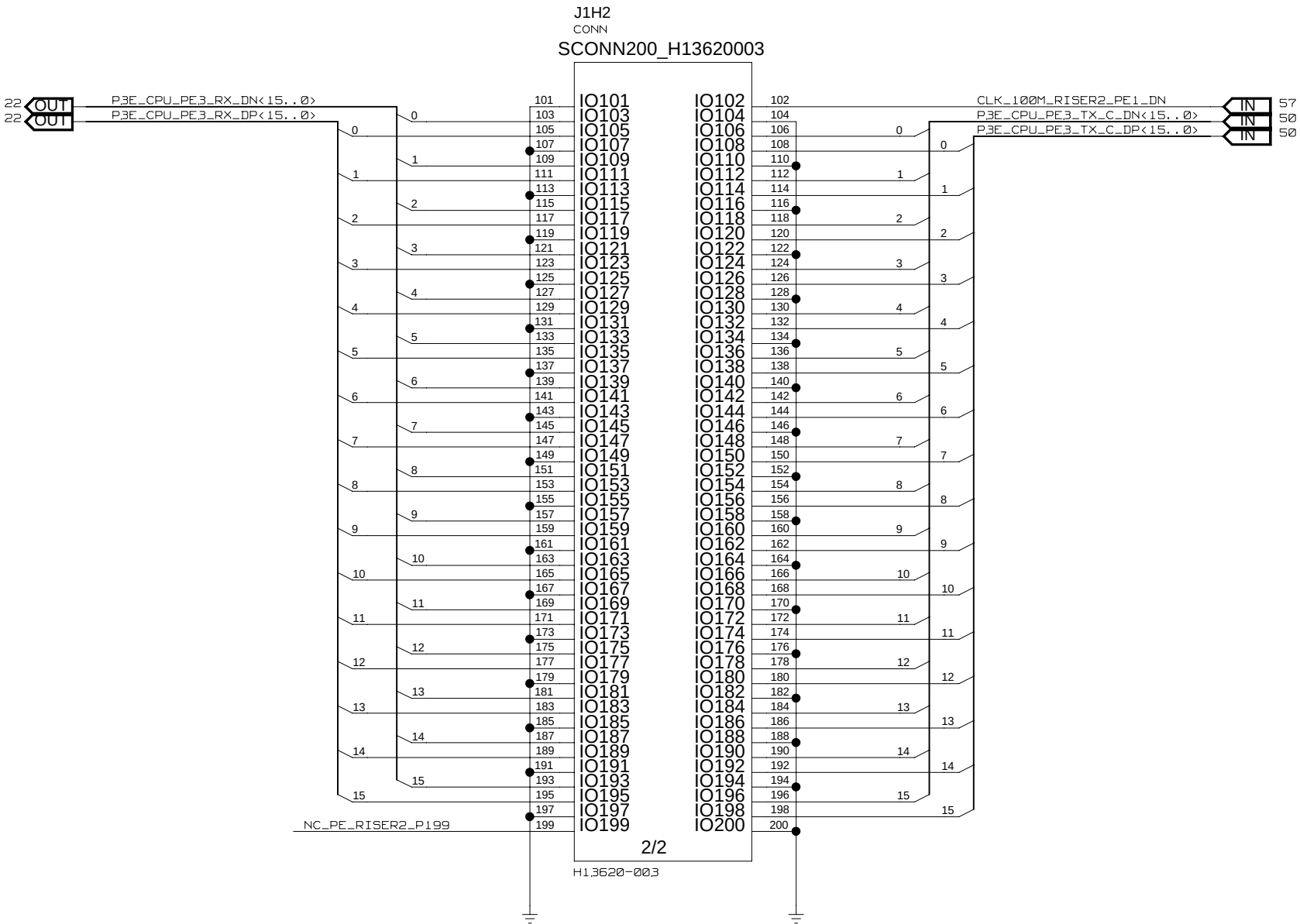
REV

3.13

SCALE:

DO NOT SCALE DRAWING

SHEET 48 OF 167



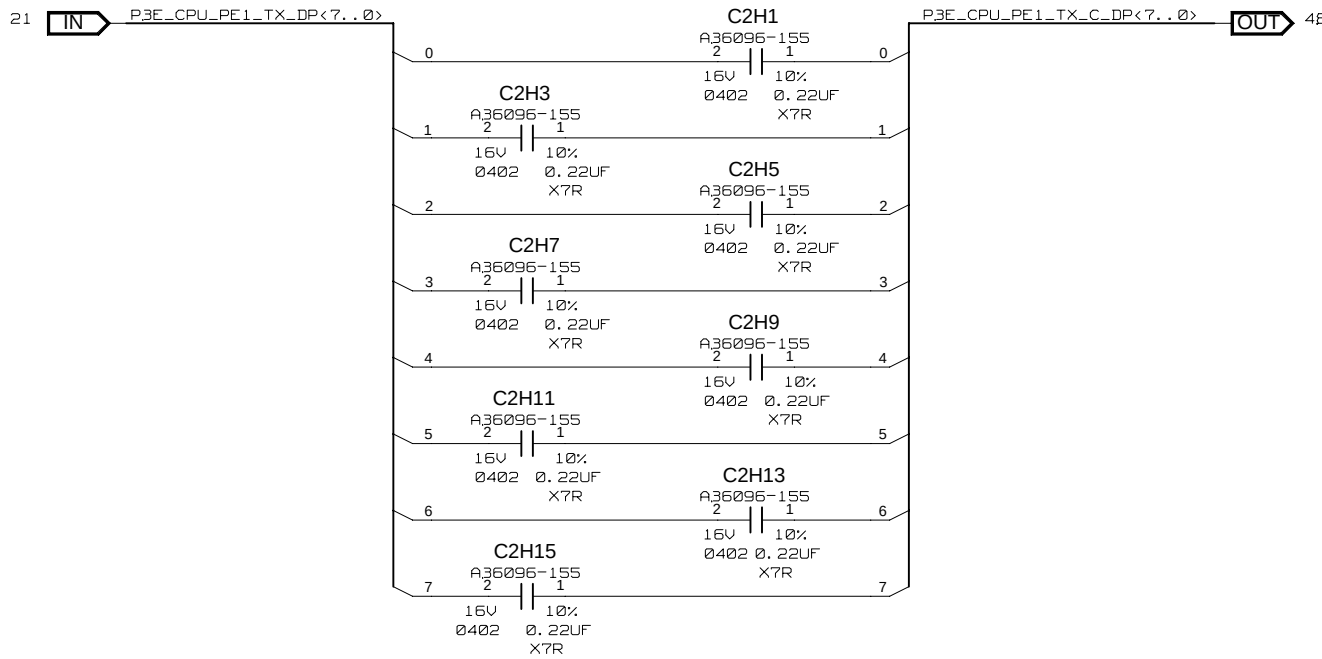
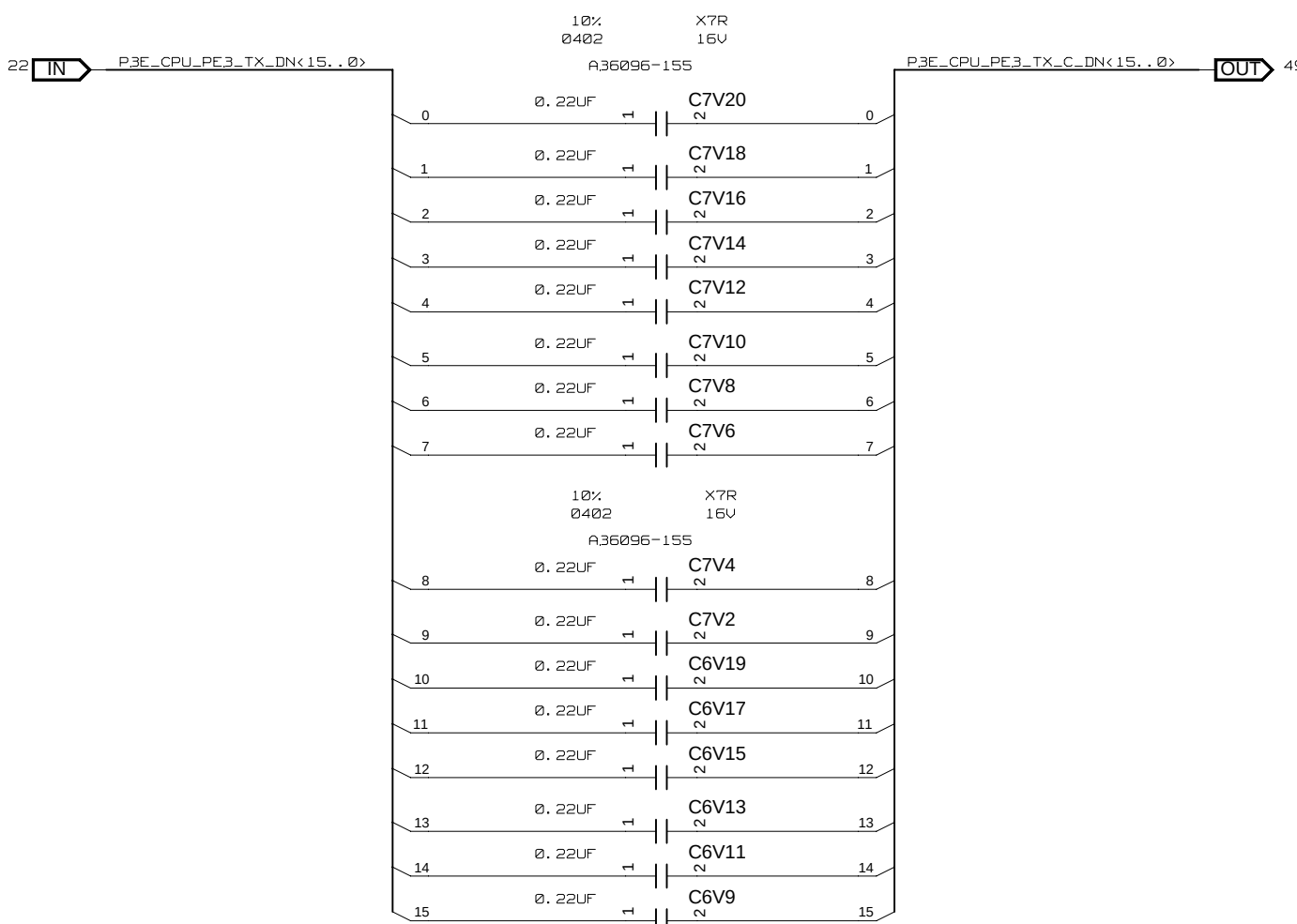
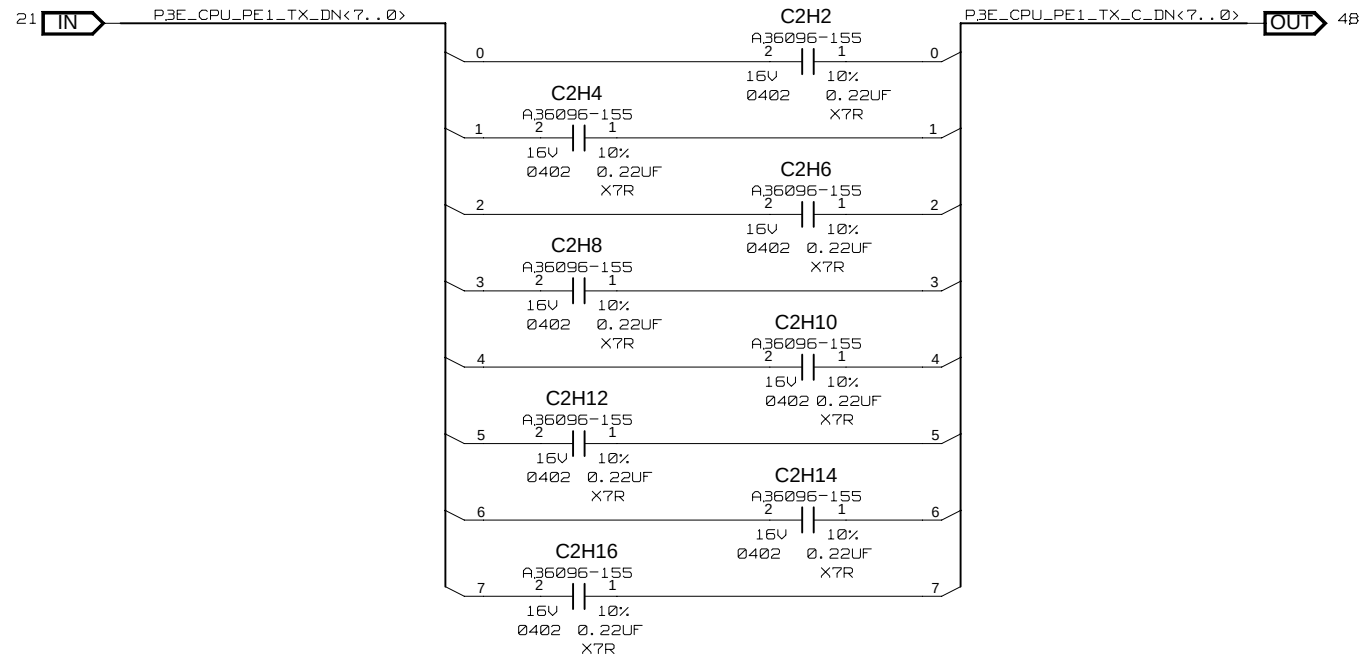
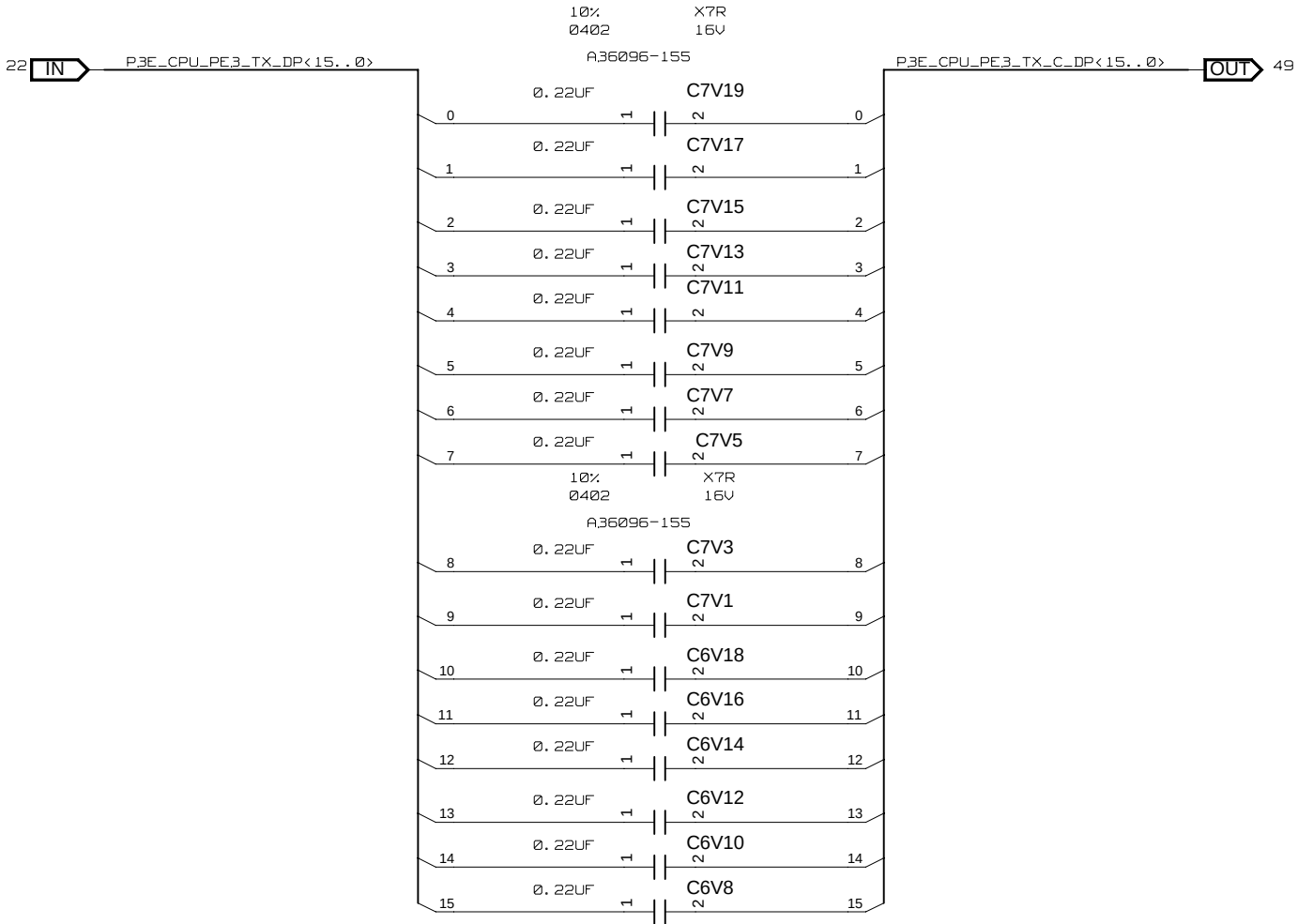
ROOM: PCIE_X24_RISER

Thu Nov 17 15:19:23 2016

DEPARTMENT	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE	CODE	DOCUMENT NUMBER		REV
CBED		B	34649	G9428608		3.13
		SCALE:	DO NOT SCALE DRAWING		SHEET 49 OF 167	

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PUT THESE CAPS NEAR X24 CONNECTOR



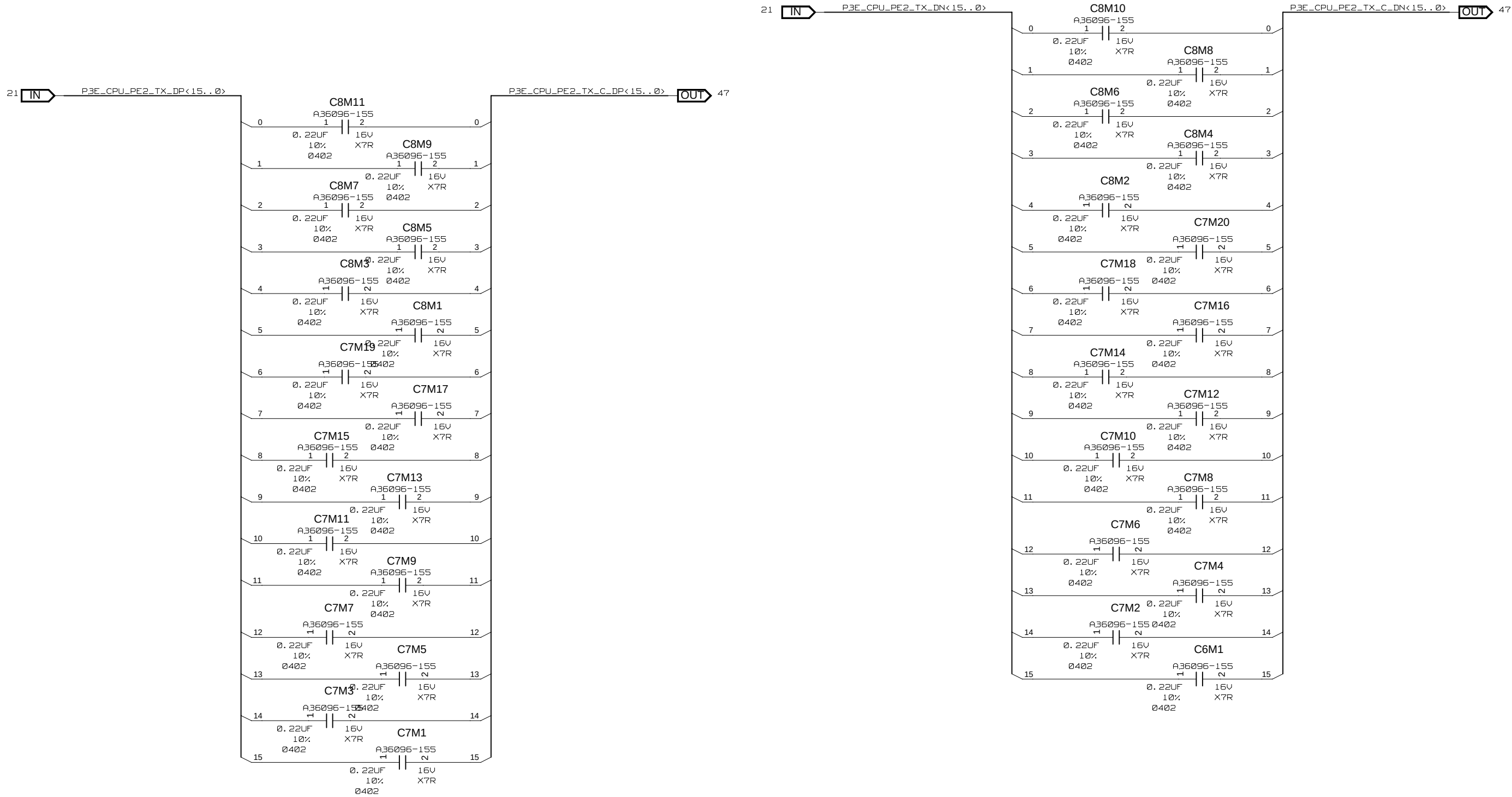
ROOM: PCIE_X24 RISER

PCIE X24 RISER AC CAPS

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		SCALE:		DO NOT SCALE DRAWING	SHEET 50 OF 167	

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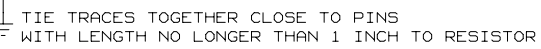


ROOM: PCIE_X16_RISER

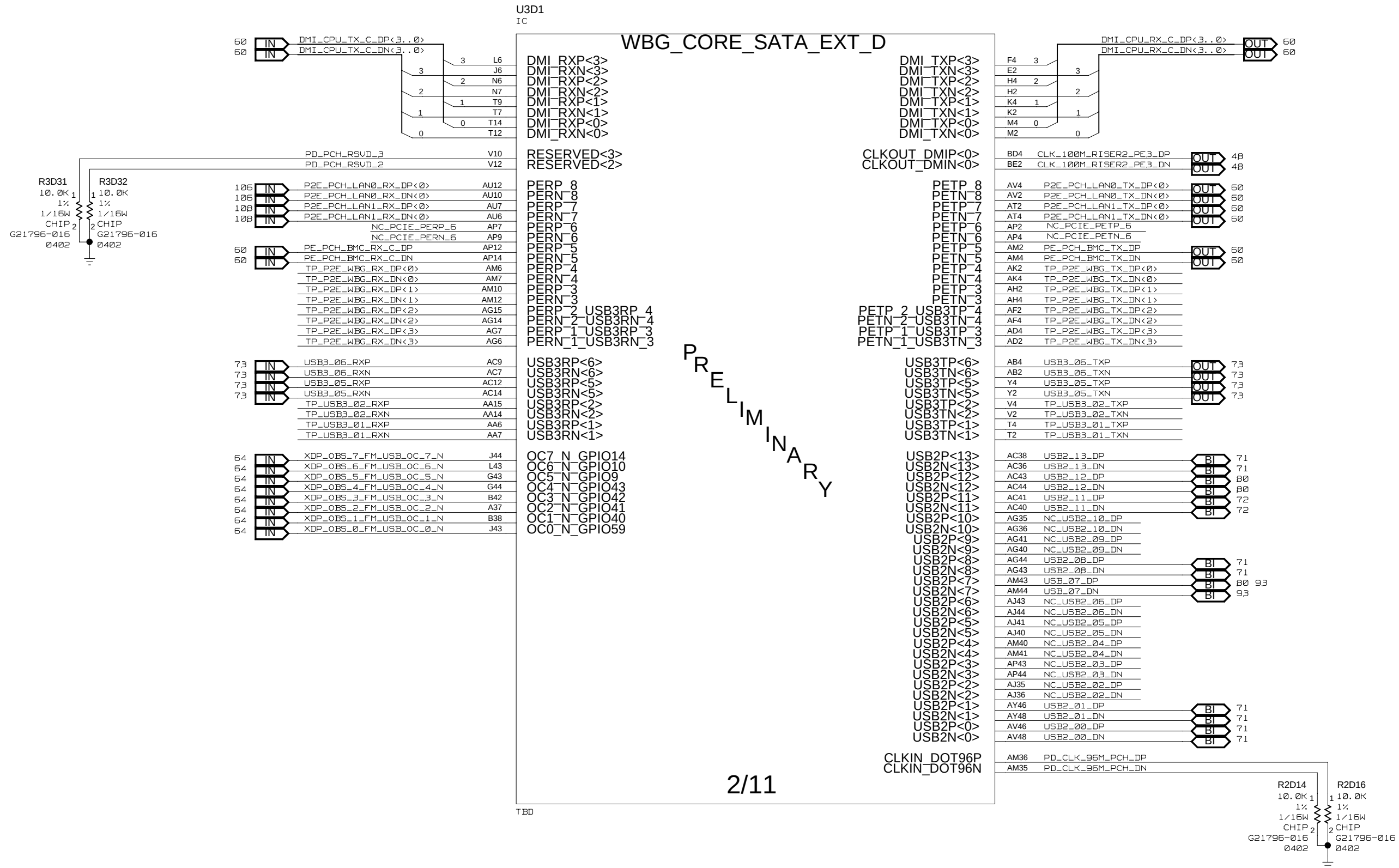
PCIE X16 RISER AC CAPS

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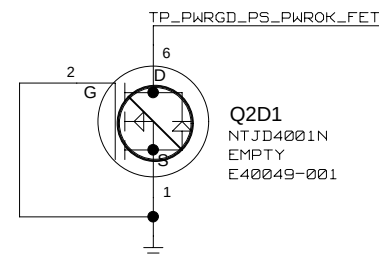
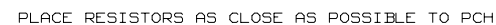
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
CBED	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	G9428608	3.13
SCALE:		DO NOT SCALE DRAWING			SHEET 51 OF 167



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B



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B

B

A

A

4

3

2

1

U3D1
IC

WBG_CORE_SATA_EXT_D



PRELIMINARY

4/11

TBD

ROOM: PCH

WBG - RESET, PWRGOOD, GPIO, SPI

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DOCUMENT NUMBER

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REV

3.13

SCALE:

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4

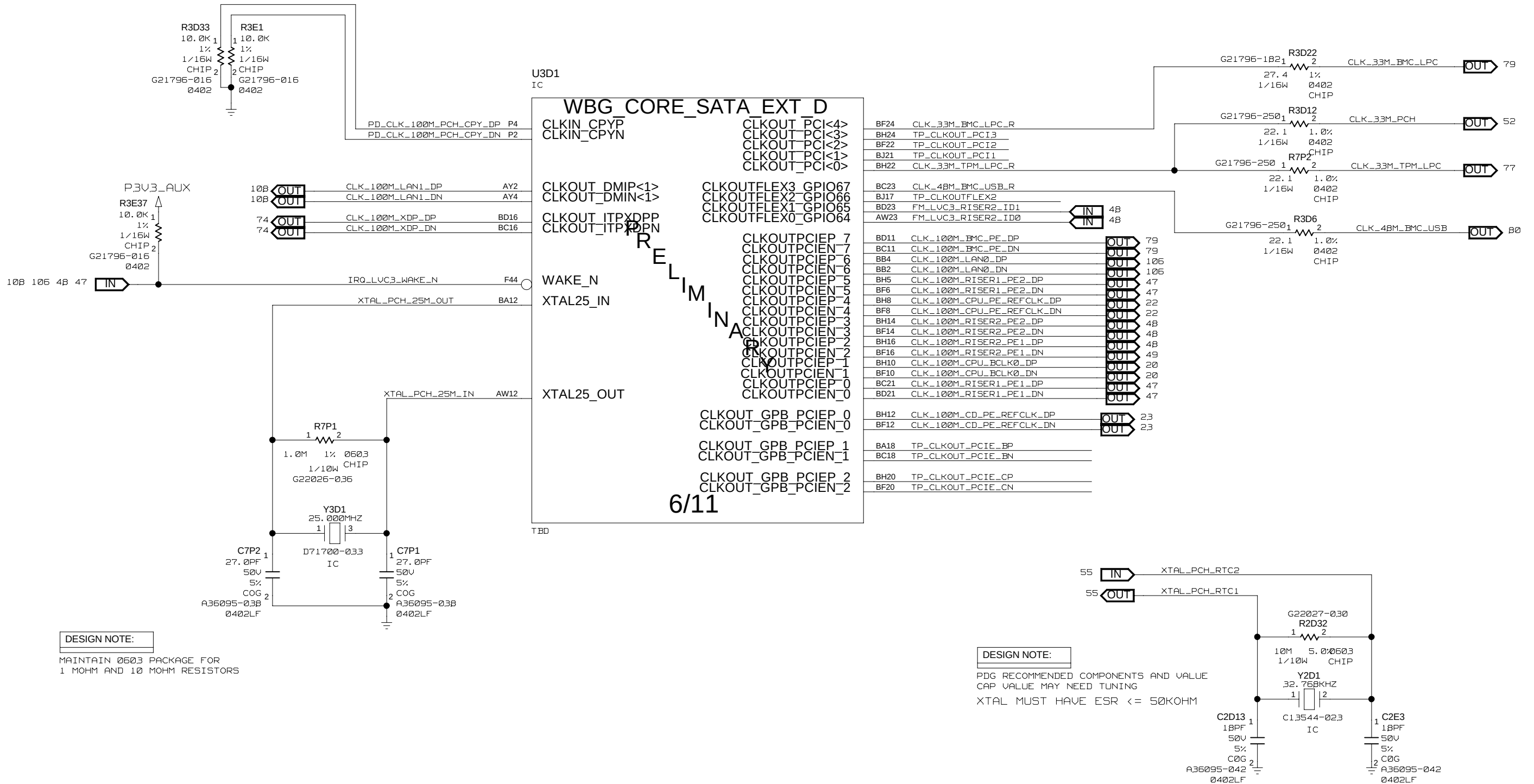
3

2

1



1



ROOM: PCH

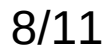
WBG - ISCLK

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
CBED	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	G9428608	3.13
SCALE:		DO NOT SCALE DRAWING			SHEET 57 OF 167

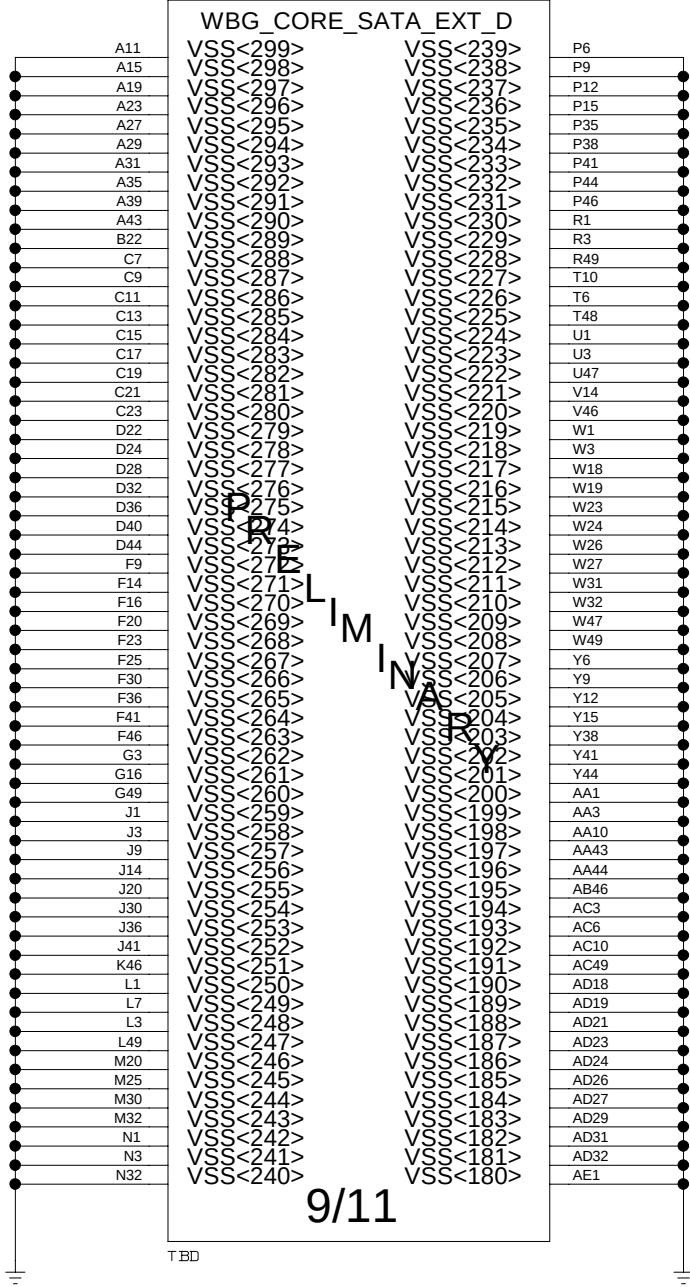
```
NOT FILTERED
STUFF: R7P7
DO NOT STUFF: R3C5

FILTERED (DEFAULT)
STUFF: R3C5
DO NOT STUFF: R7P7
```

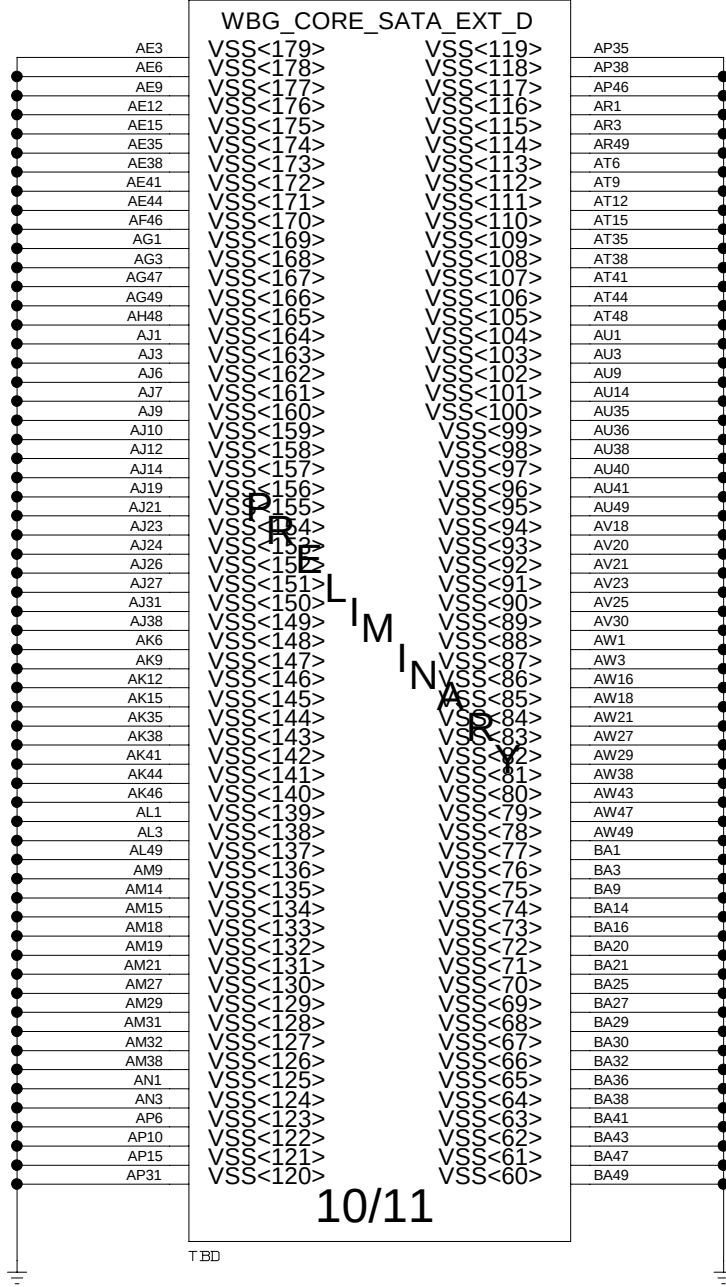


SHEET 58 OF 167

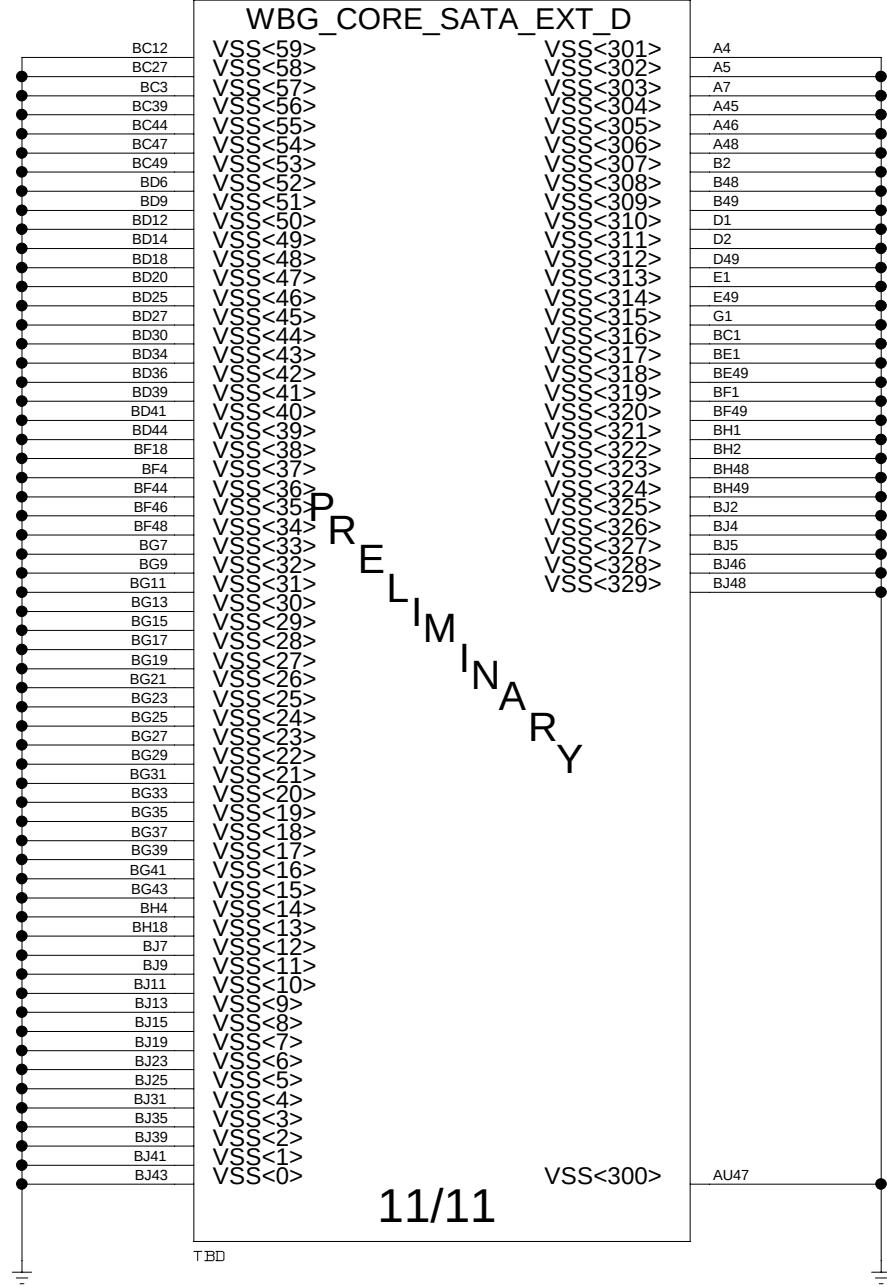
U3D1
IC



U3D1
IC



U3D1
IC



ROOM: PCH

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WBG - VSS

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DOCUMENT NUMBER

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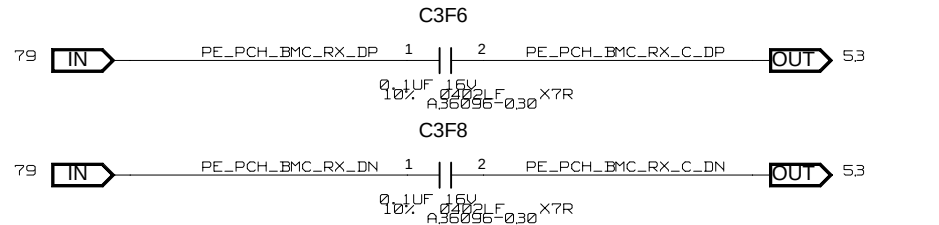
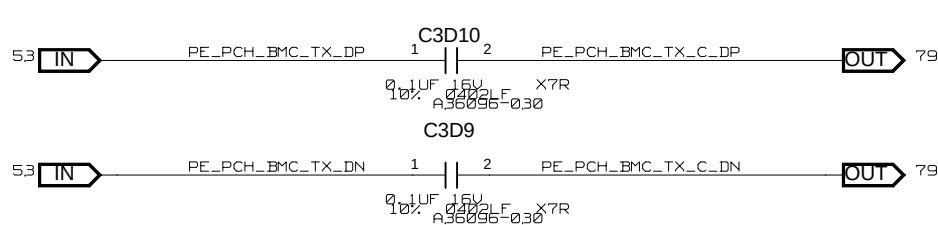
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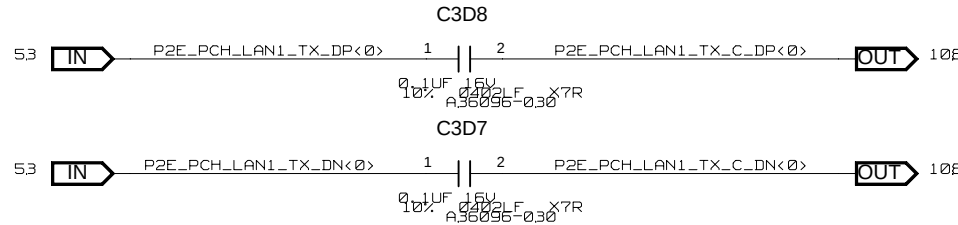
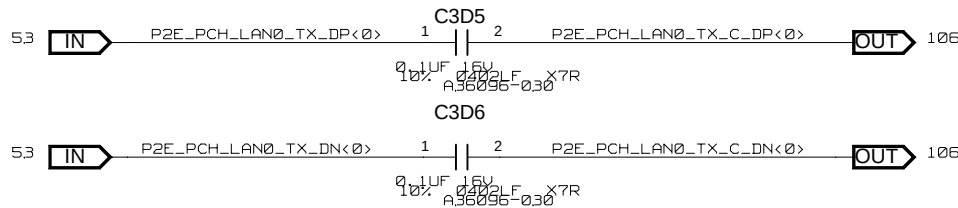
SHEET 59 OF 167

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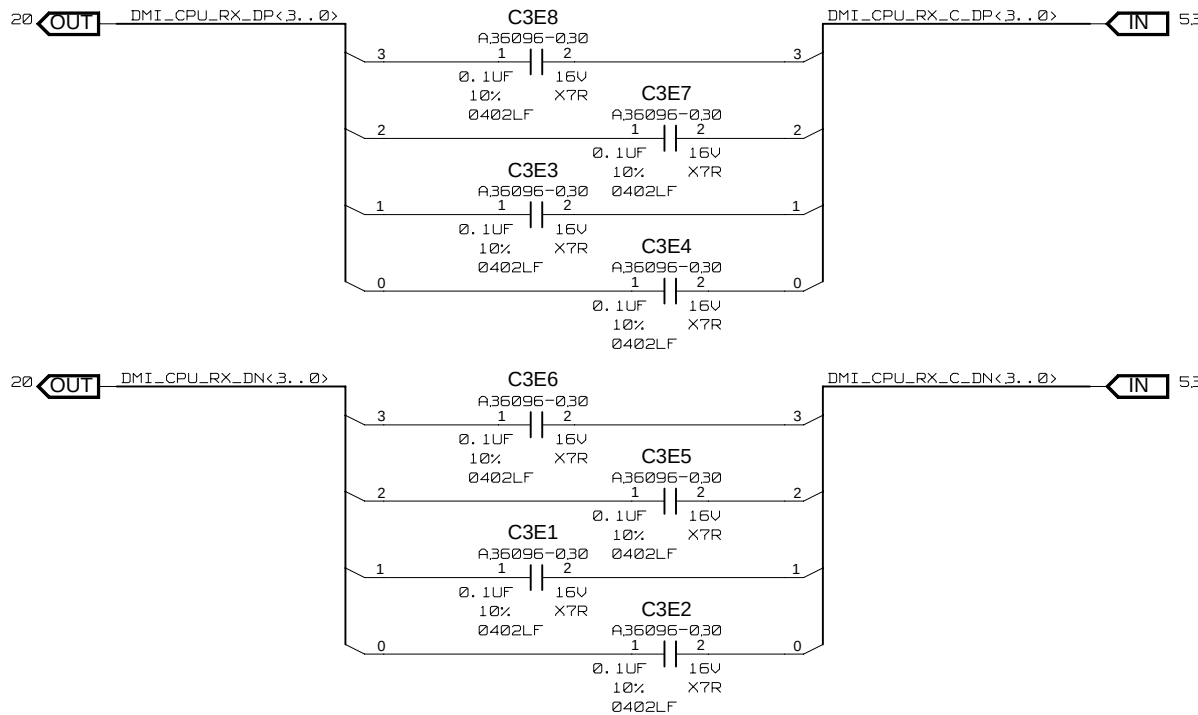
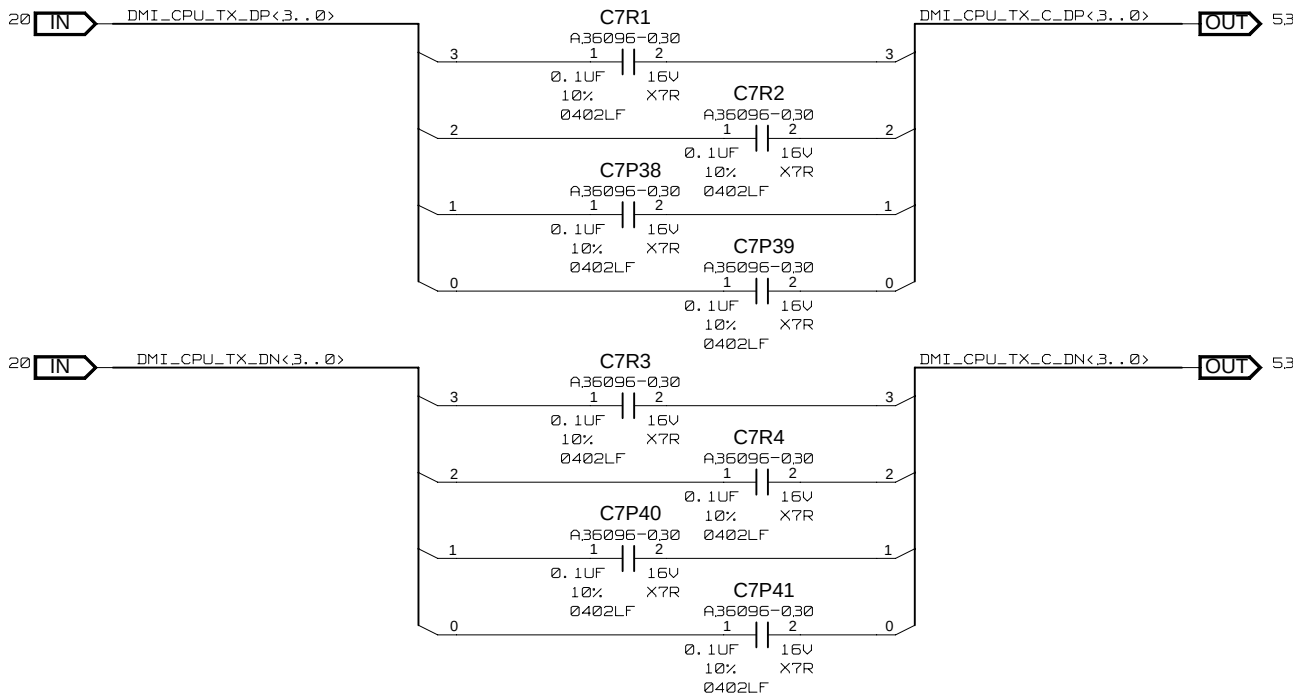
PCH BMC PCIE CAPS



PCH LAN PCIE CAPS



DMI AC CAPS



ROOM: PCH

WBG - AC CAPS

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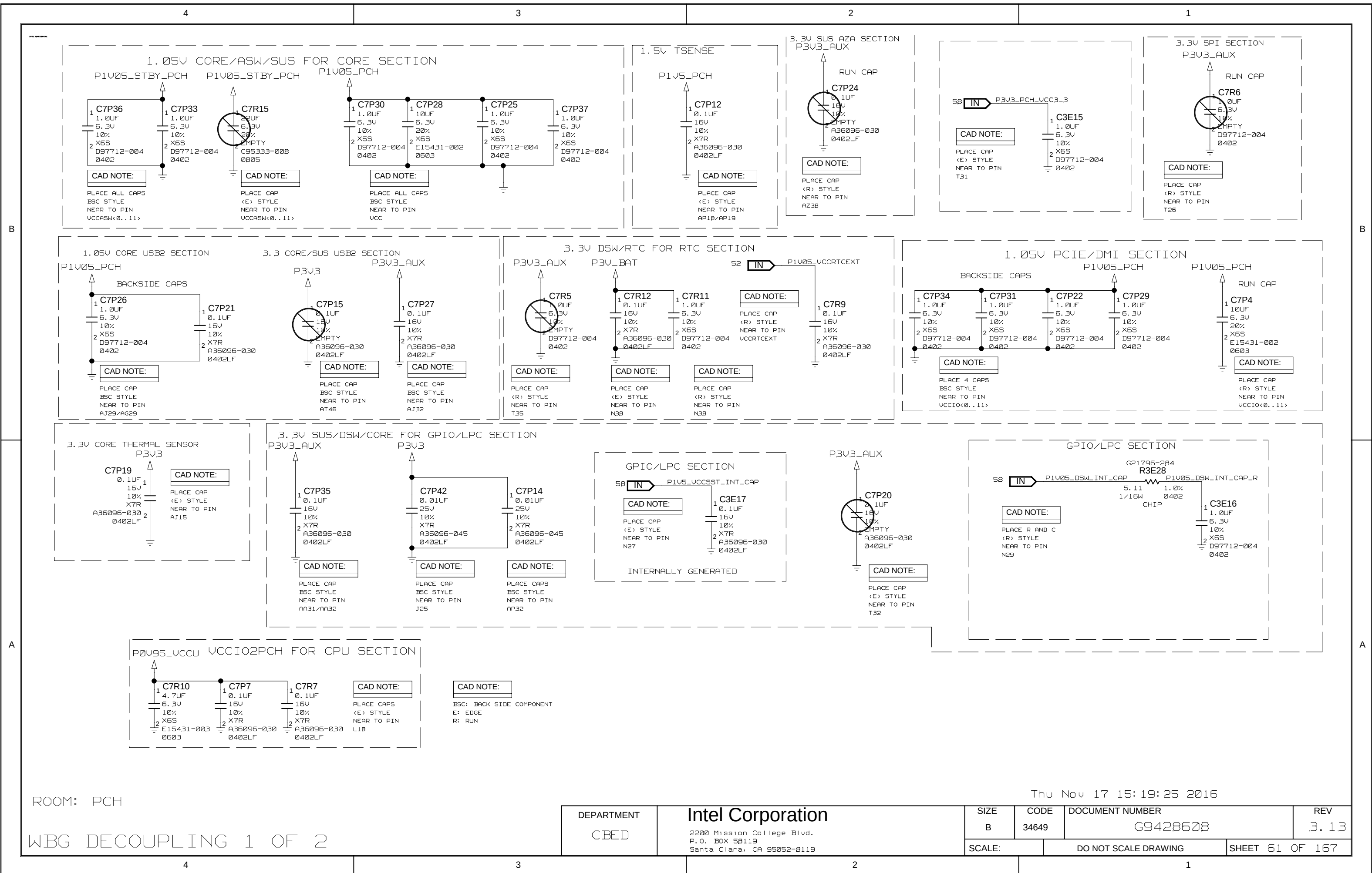
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REV
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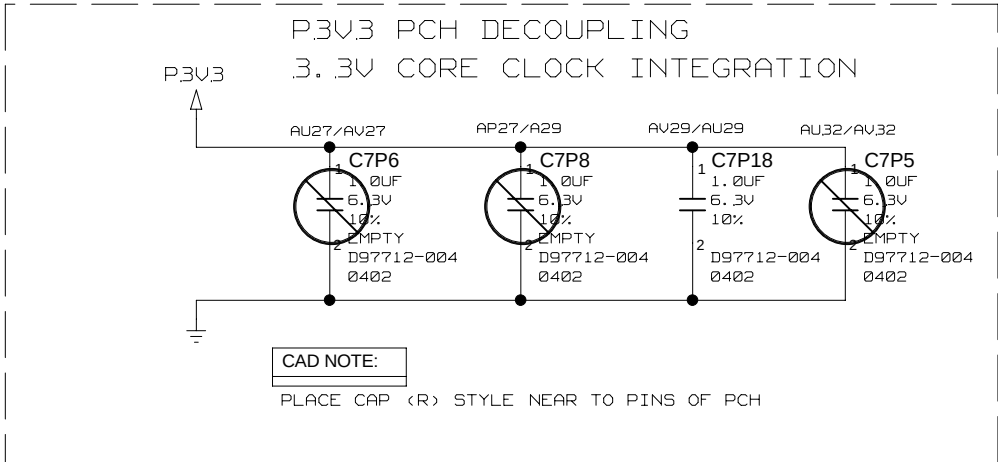
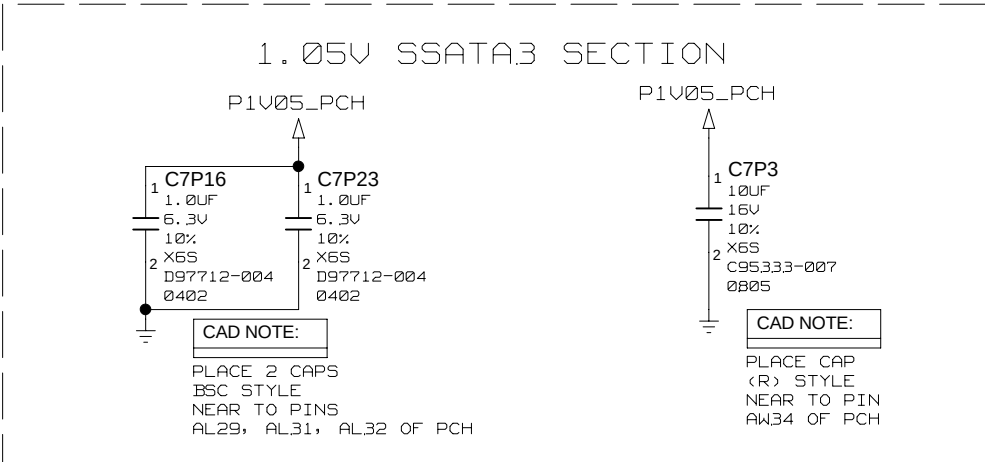
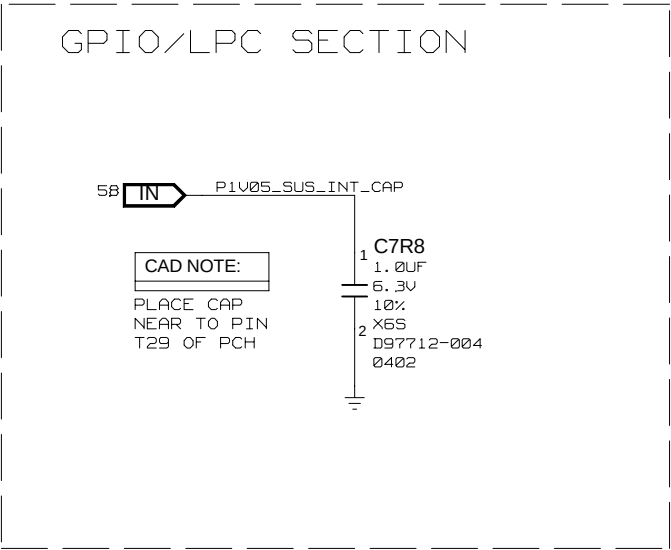
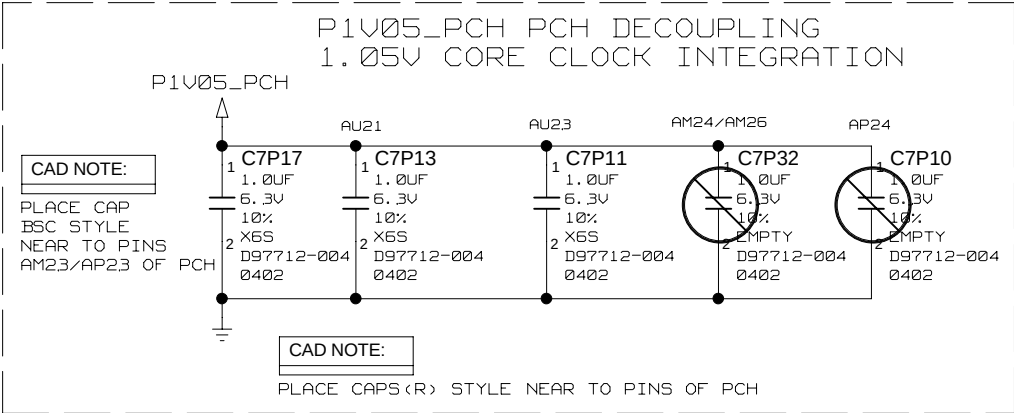
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SHEET 60 OF 167



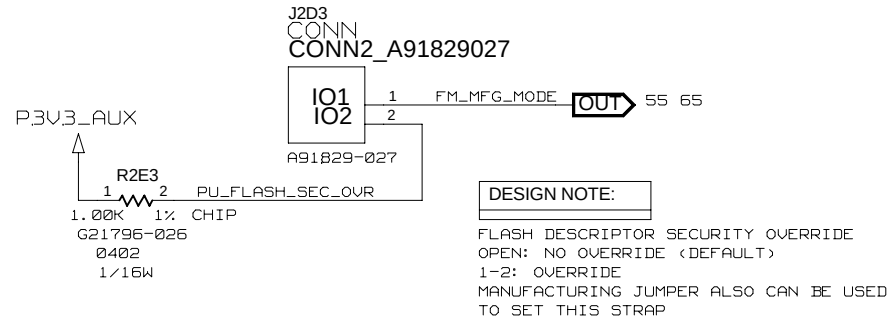
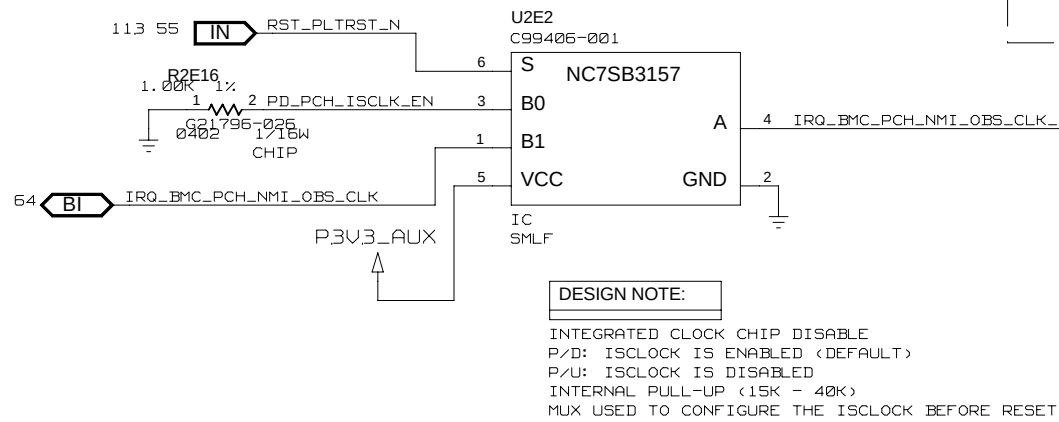
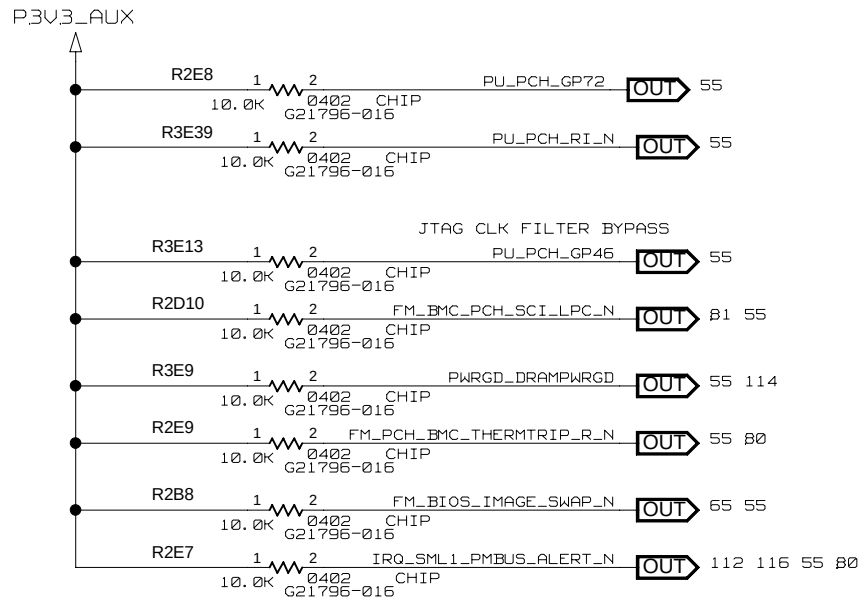
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ROOM: PCH

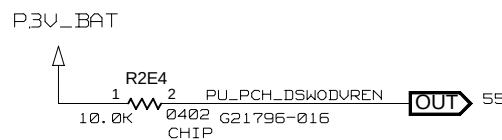
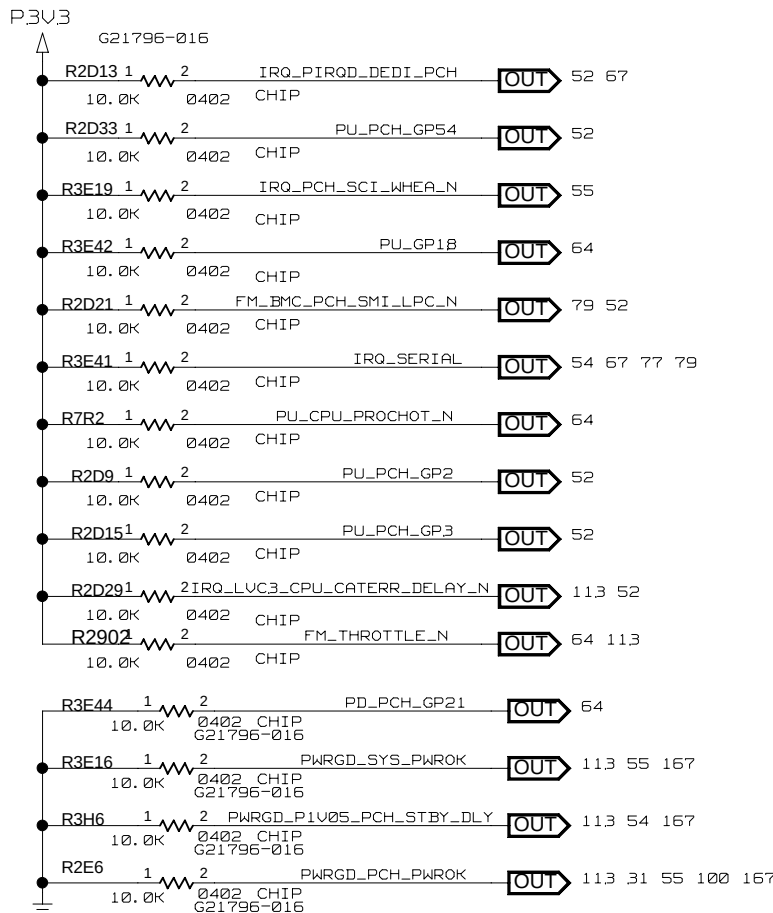
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INTEL CONFIDENTIAL



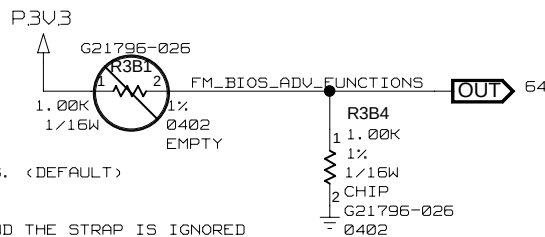
ROOM: PCH

WBG STRAPPING/MISC 1/2



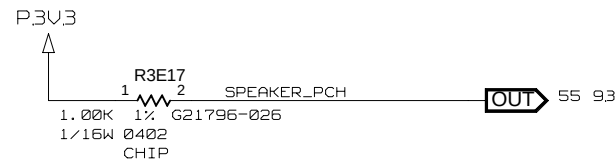
DESIGN NOTE:

DSWODVREN: DEEP SLEEP WELL ON-DIE VOLTAGE REGULATOR ENABLE
P/U: DSW ODVR IS ENABLED (DEFAULT)
P/D: DSW ODVR IS DISABLED
P/D OPTION NOT BEING PROVIDED



DESIGN NOTE:

WBG DMI RX TERMINATION
IN AC-COUPLED MODE:
0: DMI RX IS TERMINATED TO VSS. (DEFAULT)
1: OPTION NOT SUPPORTED
IN DC-COUPLED MODE:
DMI RX IS TERMINATED TO VSS AND THE STRAP IS IGNORED
INTERNAL PULL-DOWN (15K-40K)
(THE PULL-DOWN IS DIABLED AFTER PLTRST_N DEASSERTS)



DESIGN NOTE:

NO REBOOT
REBOOT DISABLE WHEN HIGH (DEFAULT)
INTERNAL PULL DOWN (15K-40K)



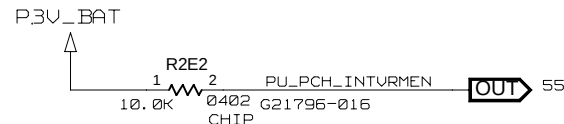
DESIGN NOTE:

WBG DMI TX TERMINATION
IN DC-COUPLED MODE:
0: DMI TX IS TERMINATED TO VSS.
1: DMI TX IS TERMINATED TO VCC.
INTERNAL PULL-DOWN (9K-50K)
WHEN OPERATING IN AC-COUPLED MODE, (DEFAULT)
THIS STRAP HAS NO EFFECT ON THE TX TERMINATION



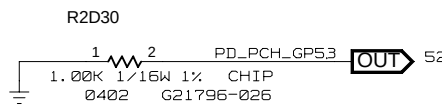
DESIGN NOTE:

TLS CONFIDENTIALITY ENABLE
P/U: TLS IS ENABLED (DEFAULT)
P/D: TLS IS DISABLED
INTERNAL PULL DOWN (15K-40K)



DESIGN NOTE:

INTERNAL VRM ENABLE: THIS SIGNAL IS USED TO ENABLE OR DISABLE THE INTEGRATED 1.05 VOLTAGE REGULATORS FOR THE SUSPEND WELL ON THE WELLSBURG
P/U: ENABLED VR (DEFAULT)
P/D: DISABLES VR
P/D OPTION NOT BEING PROVIDED



DESIGN NOTE:

DMI AC COUPLING:
0: DMI AC MODE (DEFAULT)
1: DMI DC MODE
INTERNAL PULL-UP (15K-40K)

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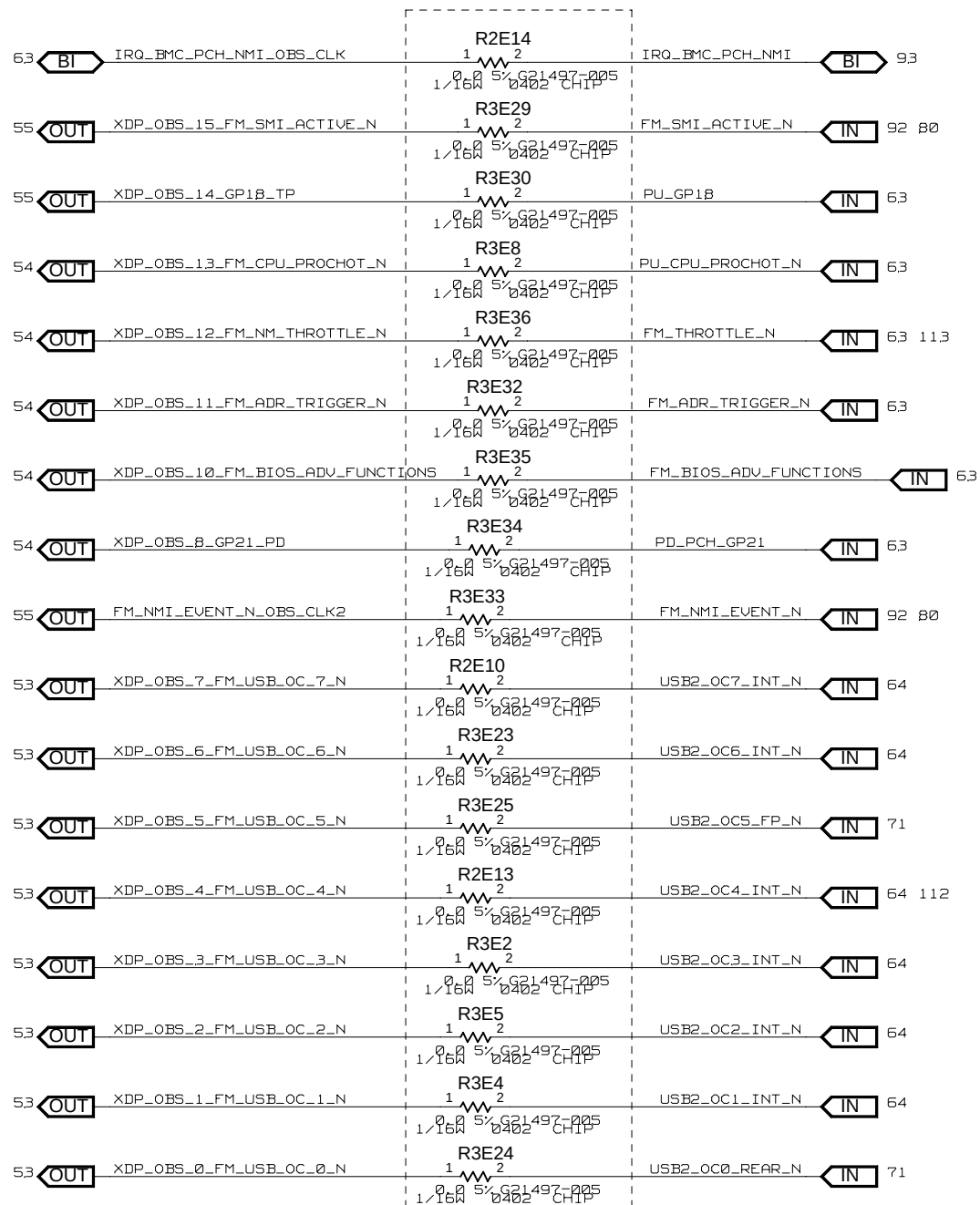
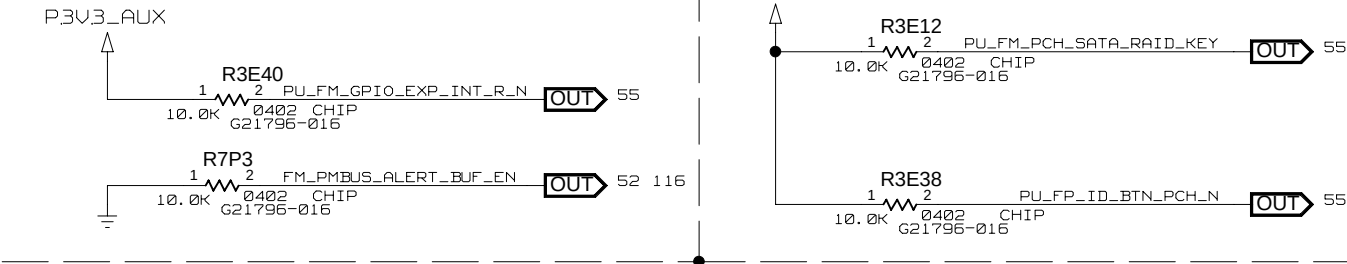
3.13

SCALE:

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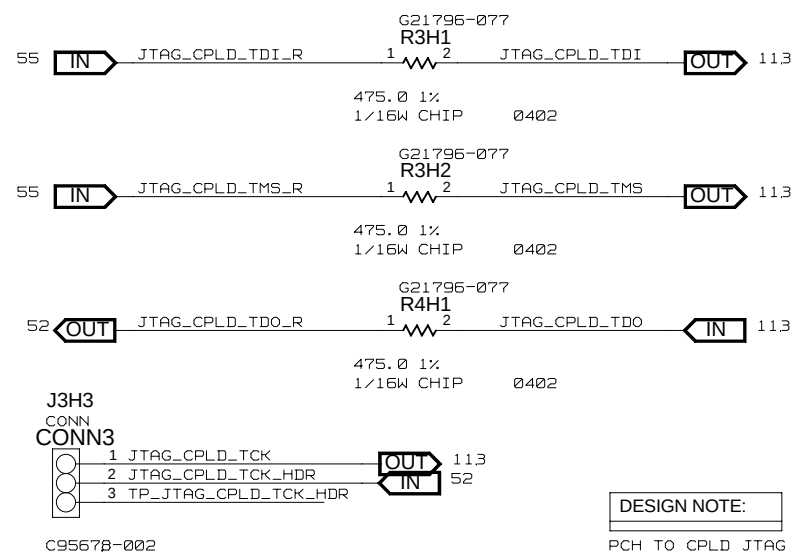
SHEET 63 OF 167

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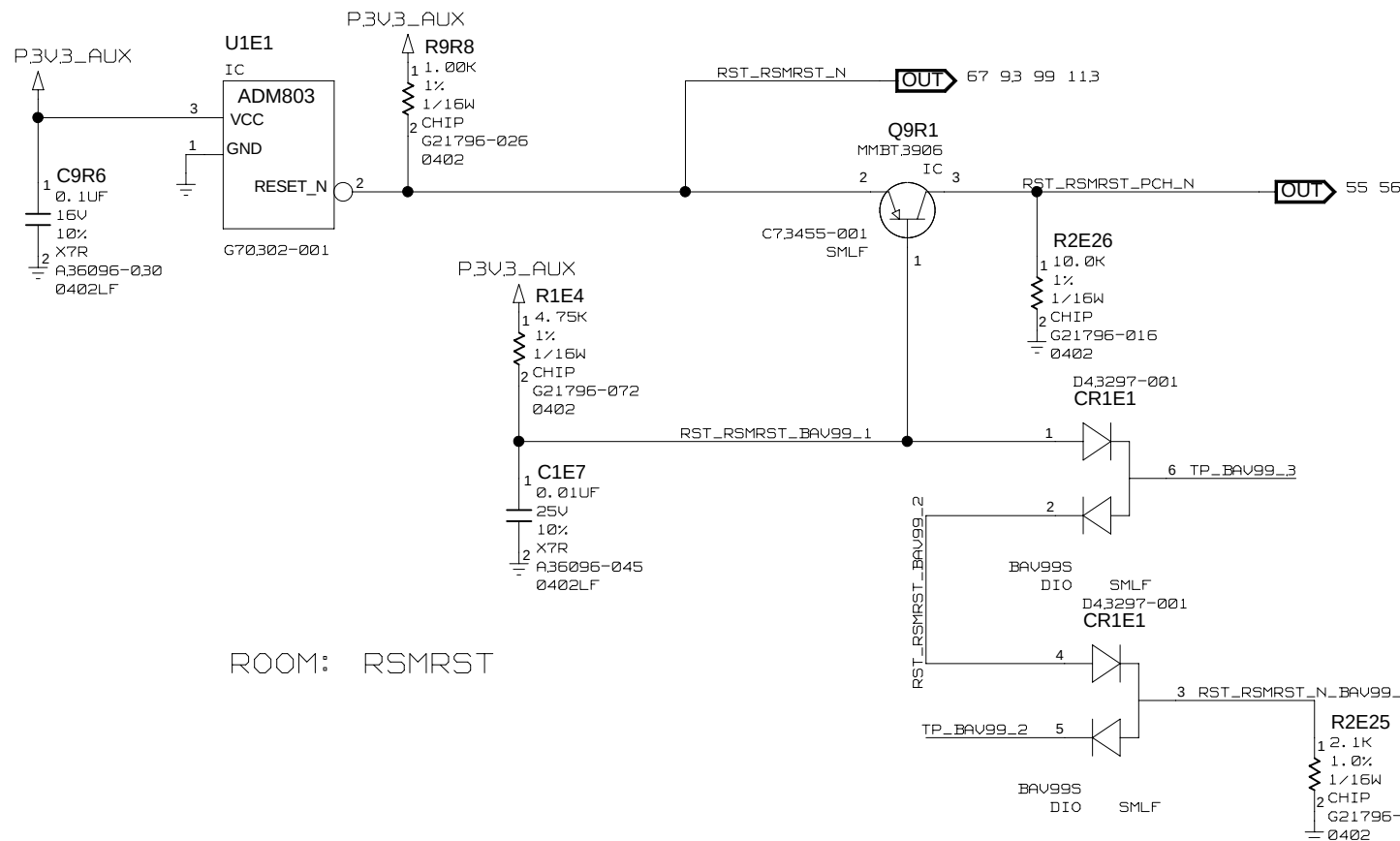


DESIGN NOTE:
REMOVE THIS RESISTORS
FOR OBSERVABILITY

PCH TO CPLD JTAG



ROOM: PCH_CPLD_JTAG



ROOM: RSMRST

ROOM: PCH

WBG STRAPPING/MISC 2/2

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SCALE:

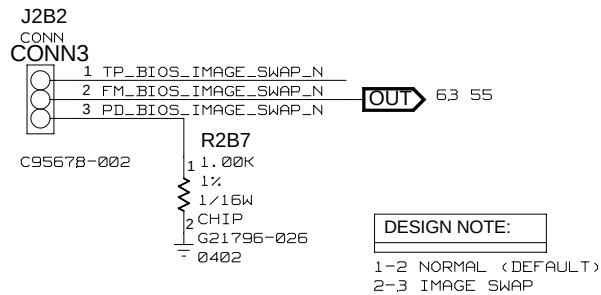
DO NOT SCALE DRAWING

SHEET 64 OF 167

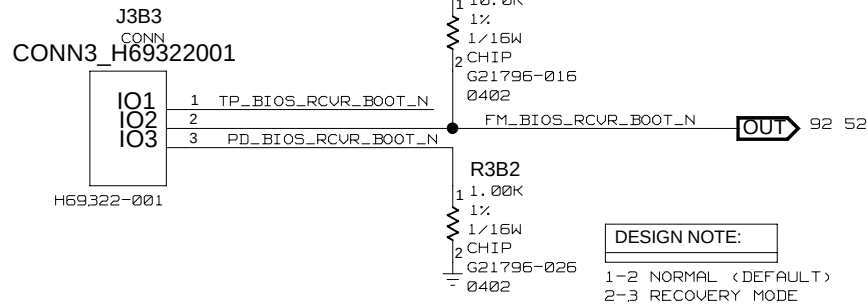
Thu Nov 17 15:19:26 2016

INTEL CONFIDENTIAL

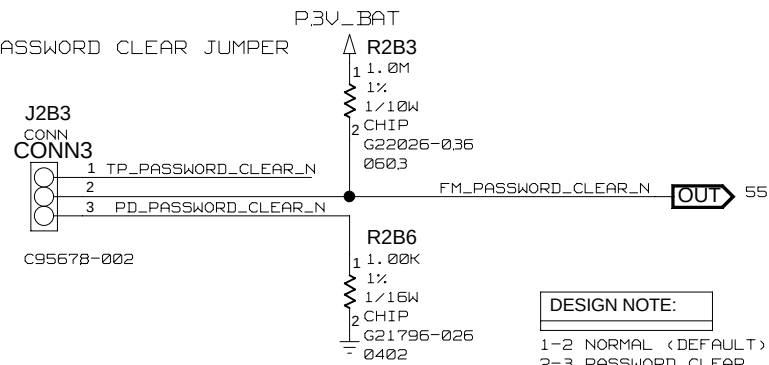
BIOS IMAGE SWAP JUMPER



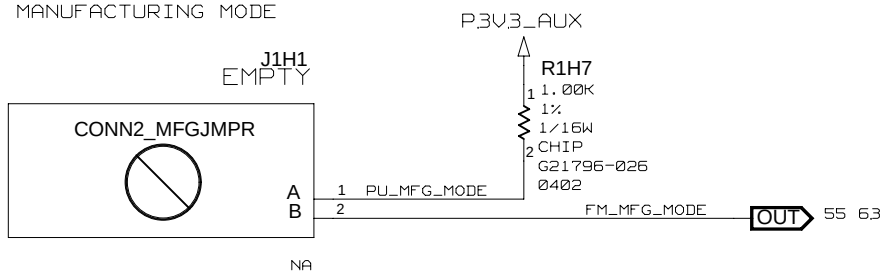
BIOS RECOVERY MODE JUMPER



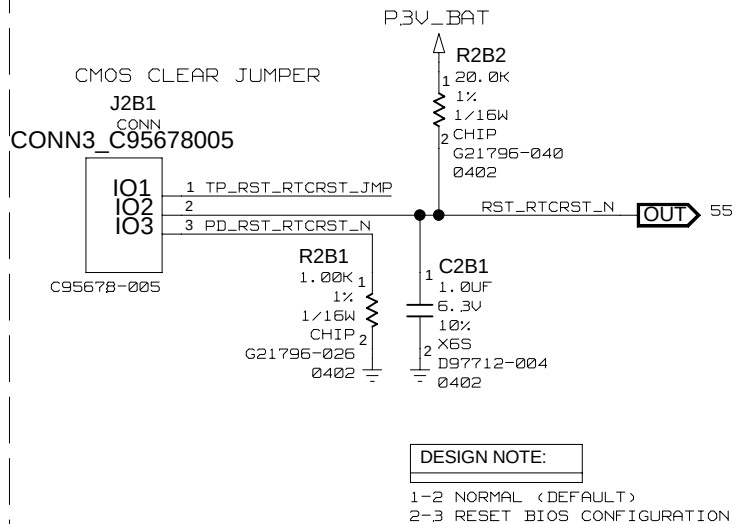
PASSWORD CLEAR JUMPER



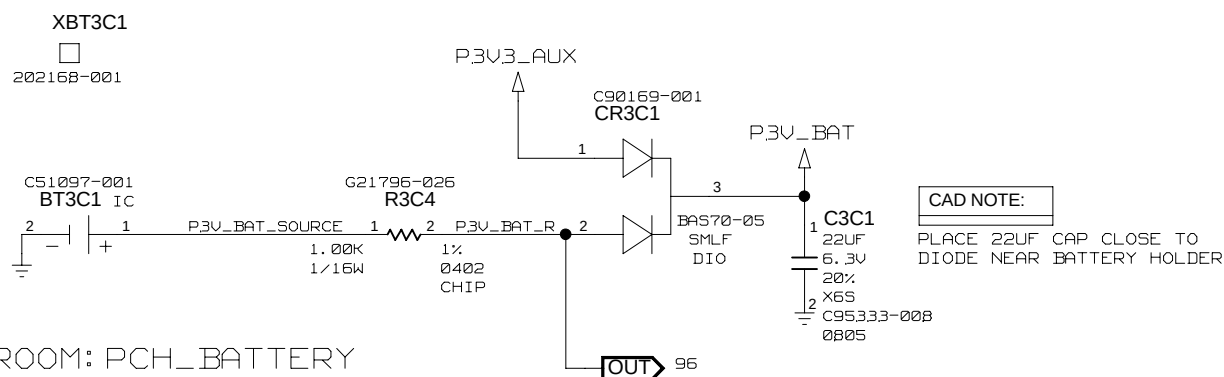
MANUFACTURING MODE



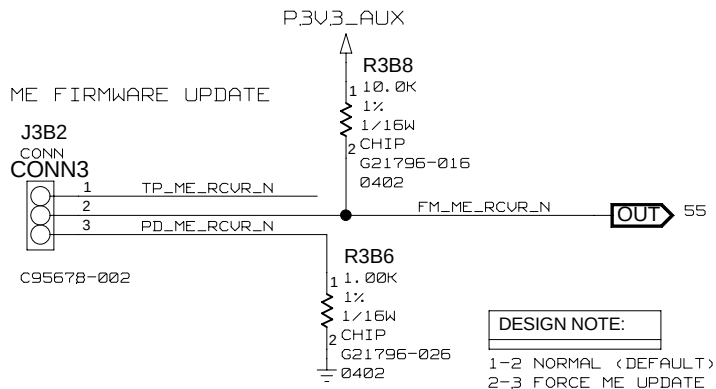
CMOS CLEAR JUMPER



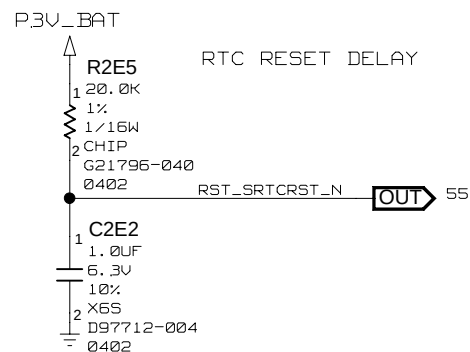
COIN TYPE BATTERY



ME FIRMWARE UPDATE



RTC RESET DELAY



ROOM: PCH

WBG HEADERS

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REV

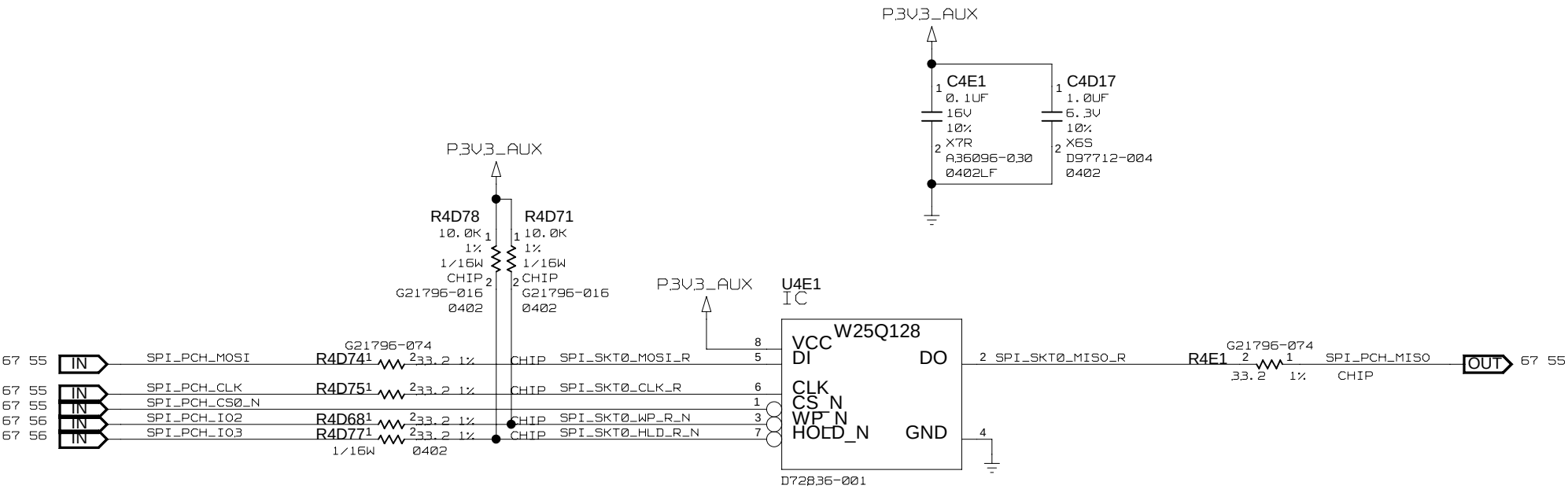
.3.13

SCALE:

DO NOT SCALE DRAWING

SHEET 65 OF 167

BIOS FLASH



BOM NOTE:

16MB FLASH IPN: G76.330-001
WINBOND W25Q128FVSIQ

BOM NOTE:

SOCKET IS D728.36-001
SOCKET WILL BE REMOVED FOR HVM

BOM NOTE:

REPLACE WITH PROGRAMMED PART
H79512-006 IN BOM

ROOM: PCH_SPI

WBG SPI FLASH

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PLACE AND MARK DEDIPROG HEADER
CLOSE TO THE BIOS FLASH SOCKET.

FOLLOW RECOMMENDED PDG TOPOLOGY



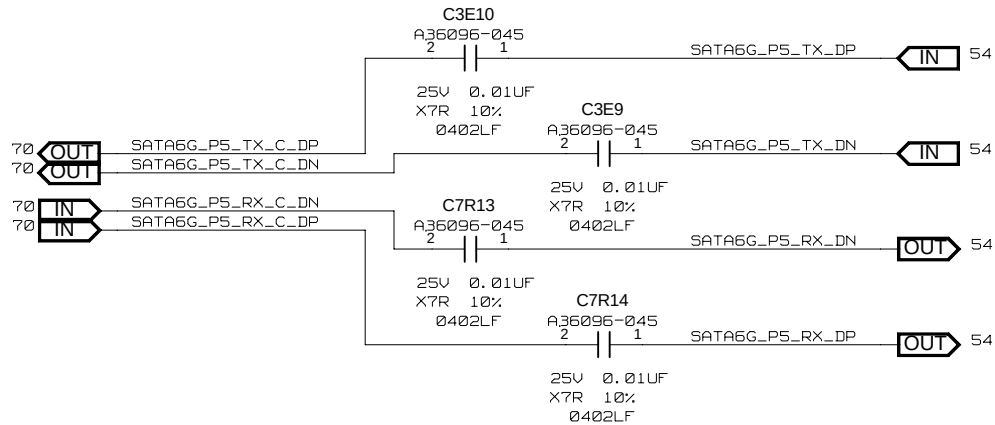
PLACE AND MARK THESE PU AND PD IN SUCH
WAY AS TO EASILY LOCATE THEM FOR REWORK.

PU STUFFED: NOT WRITE-PROTECTED (DEFAULT).
PD STUFFED: WRITE PROTECTED.

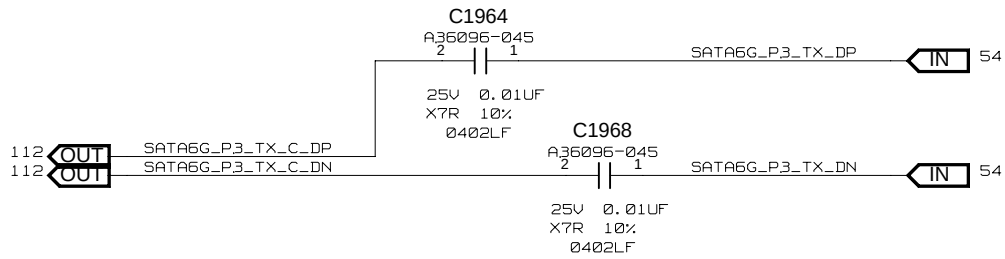
Thu Nov 17 15:19:26 2016

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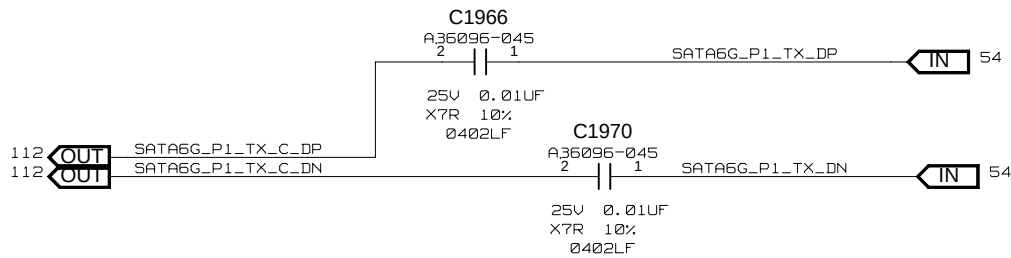
SATA PORT 5



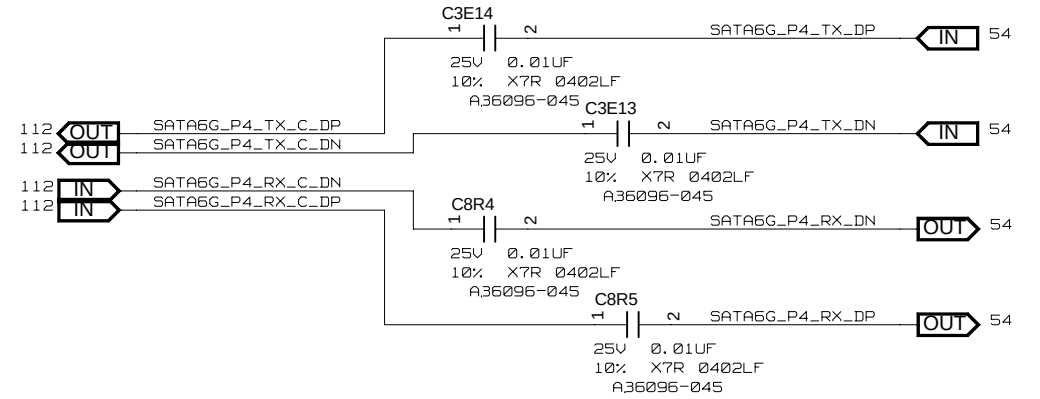
SATA PORT 3



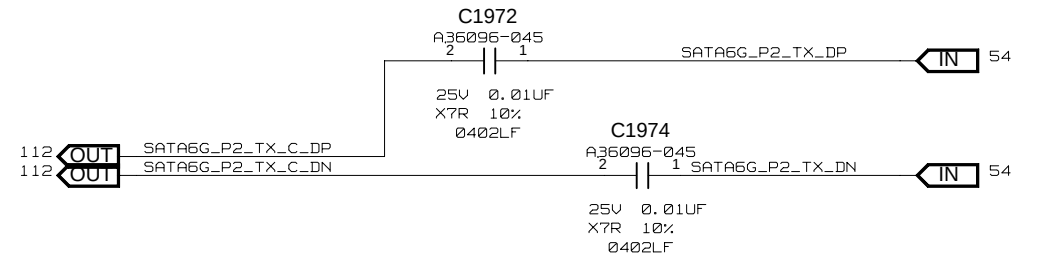
SATA PORT 1



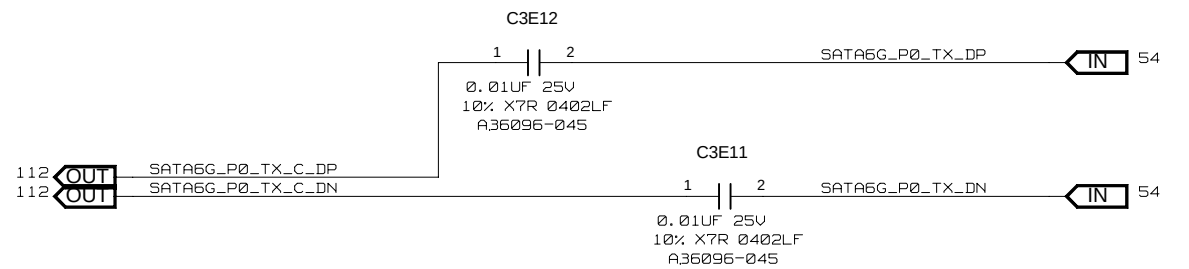
SATA PORT 4



SATA PORT 2



SATA PORT 0



ROOM: SATA_CONNECTORS

SATA AC CAPS

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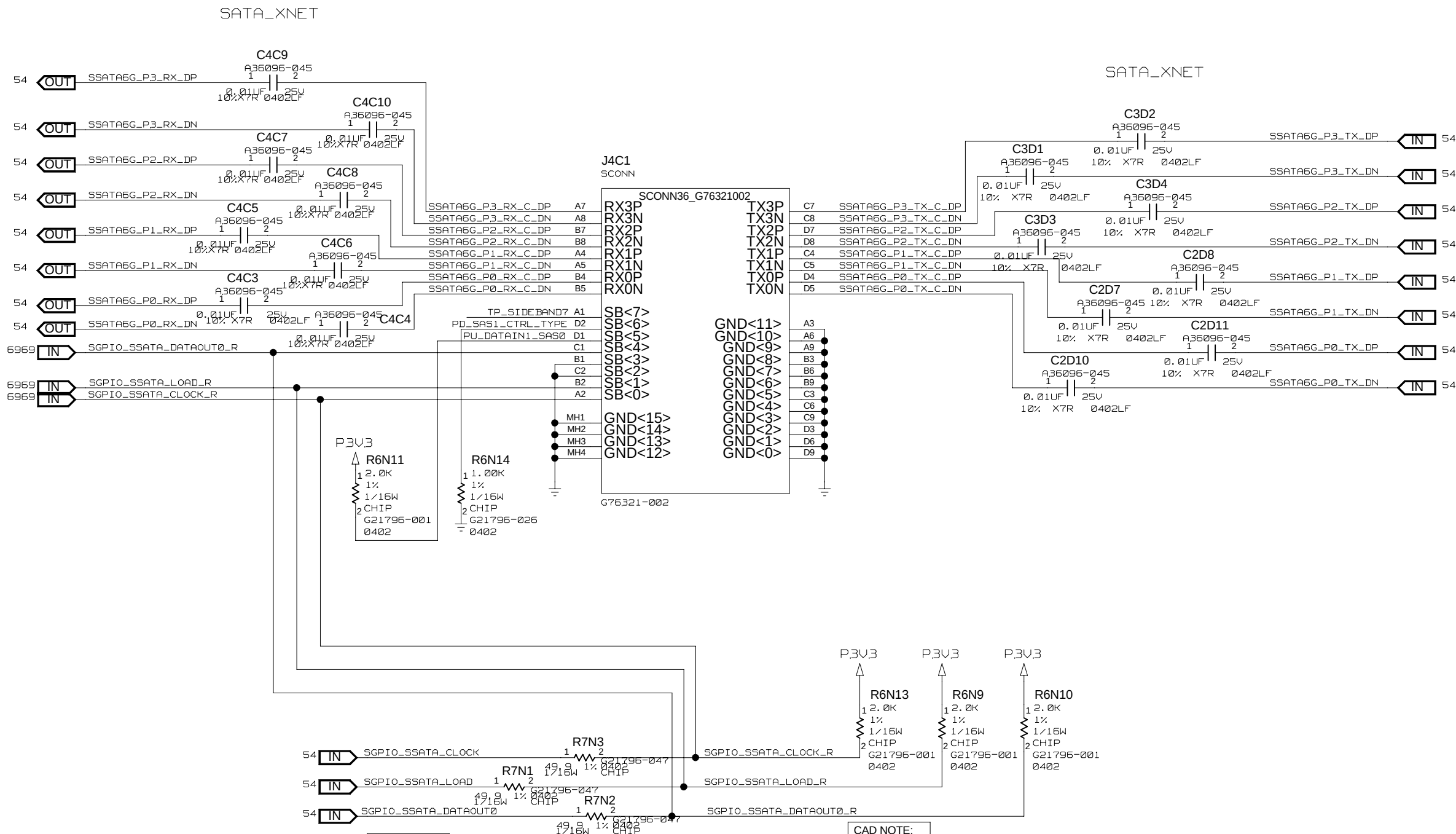
.3.13

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SSATA PORTS 0 THROUGH 3. G3 @6.0 GBPS

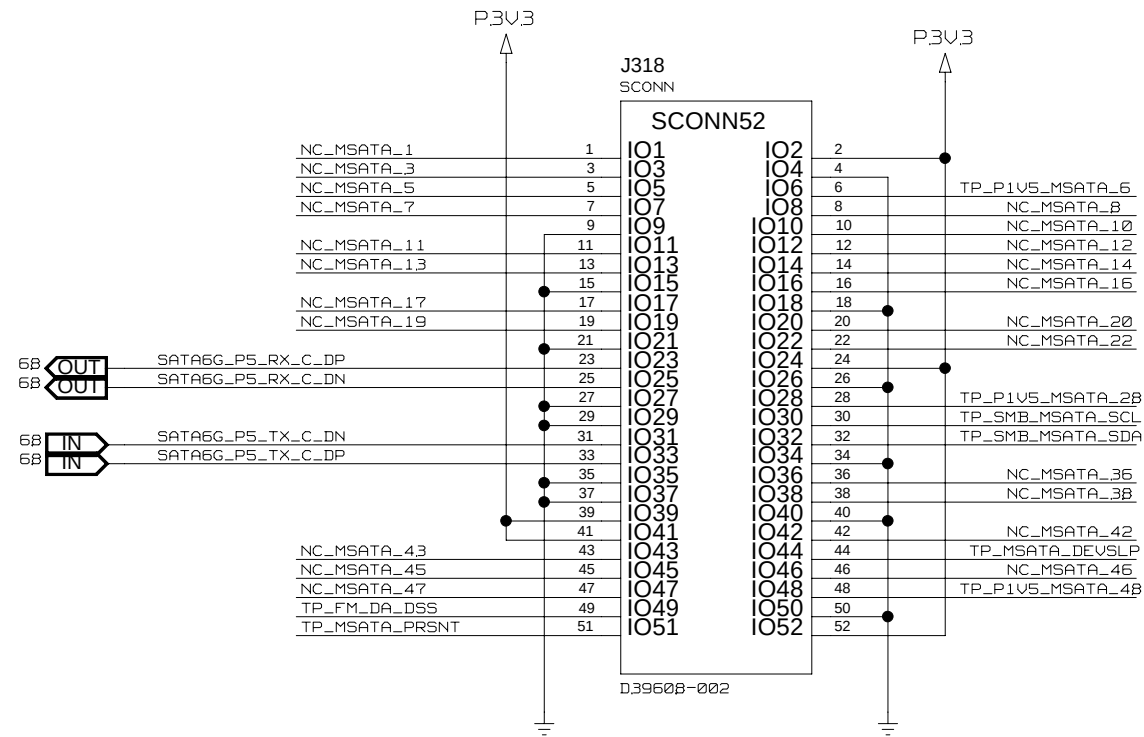


ROOM: WBG_SSATA_CONN

S-SATA CONNECTOR

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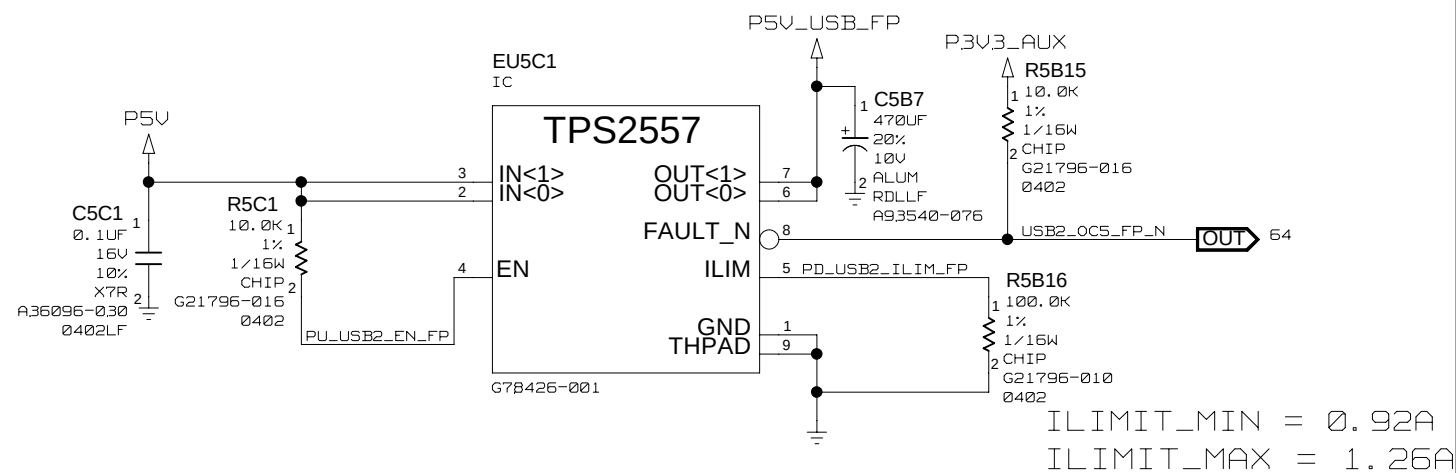
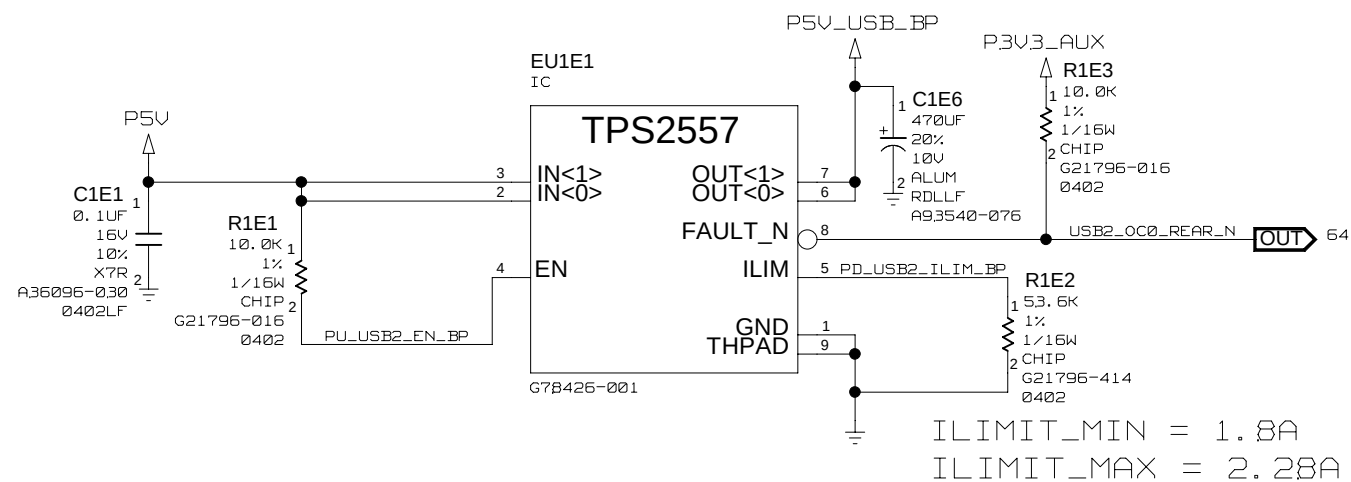
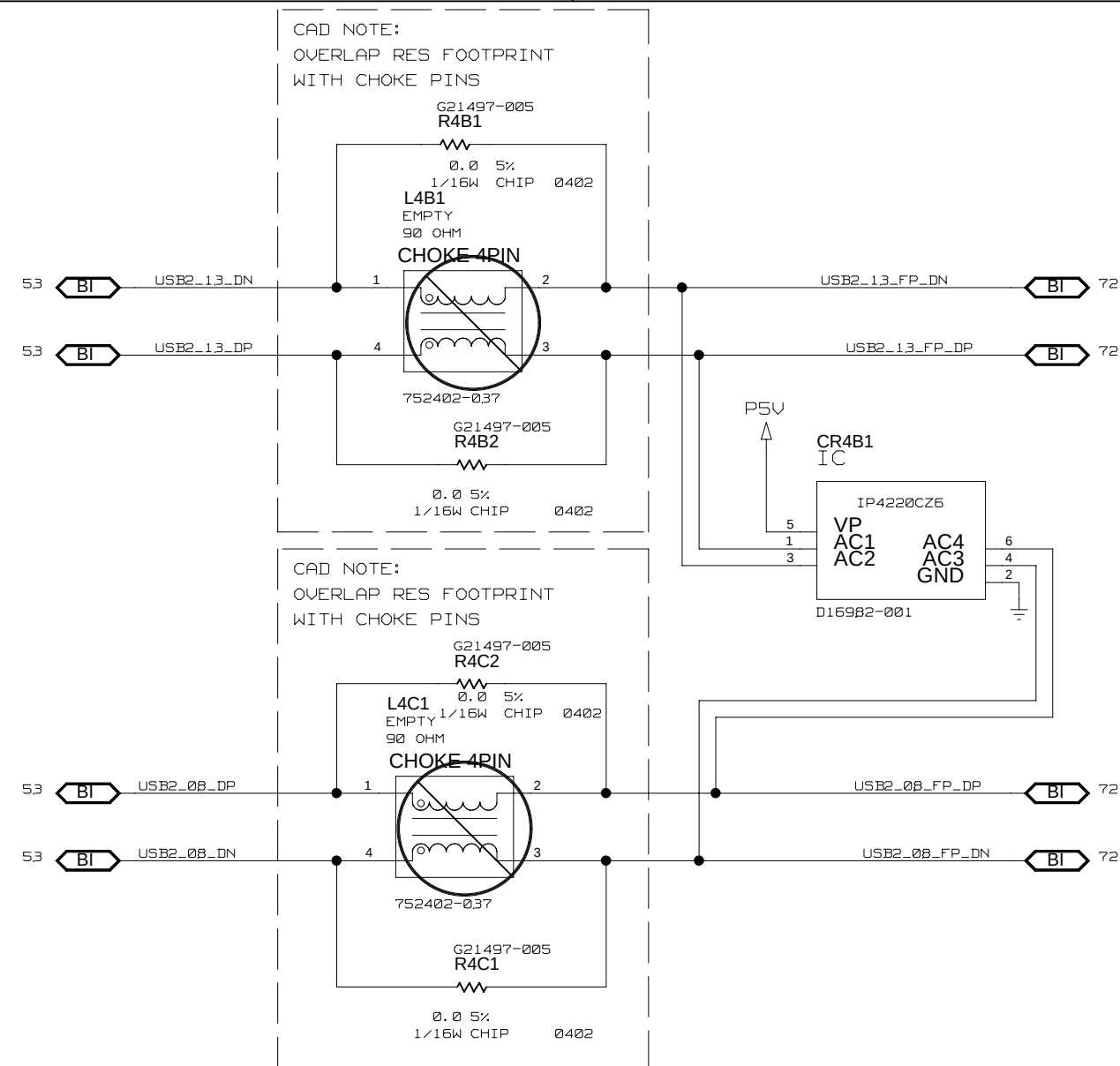
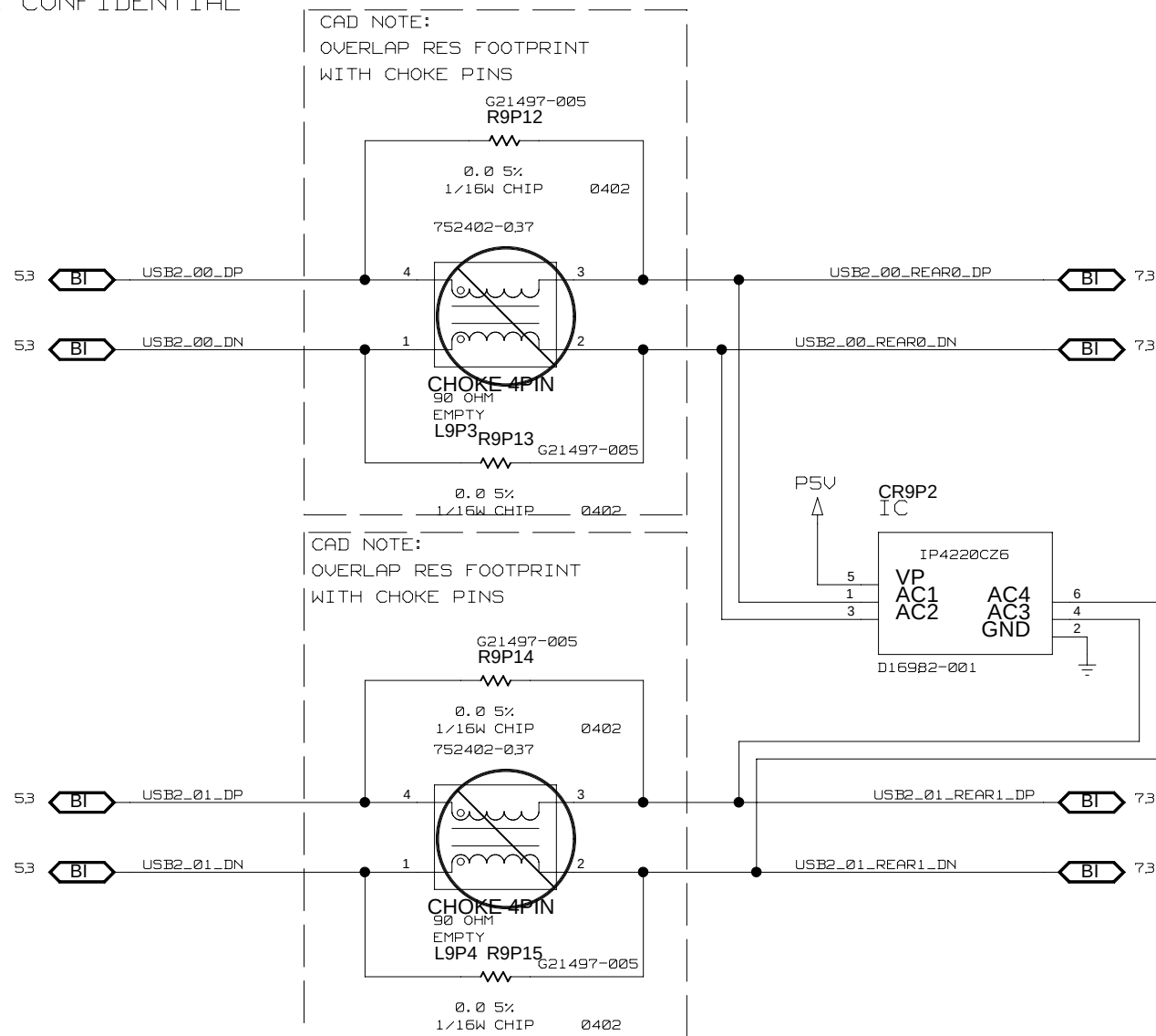
ROOM: MSATA

MSATA CONNECTOR

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ROOM: BP_USB_CONN
BOM_COST: MIO_USB

USB2 CONNECTORS

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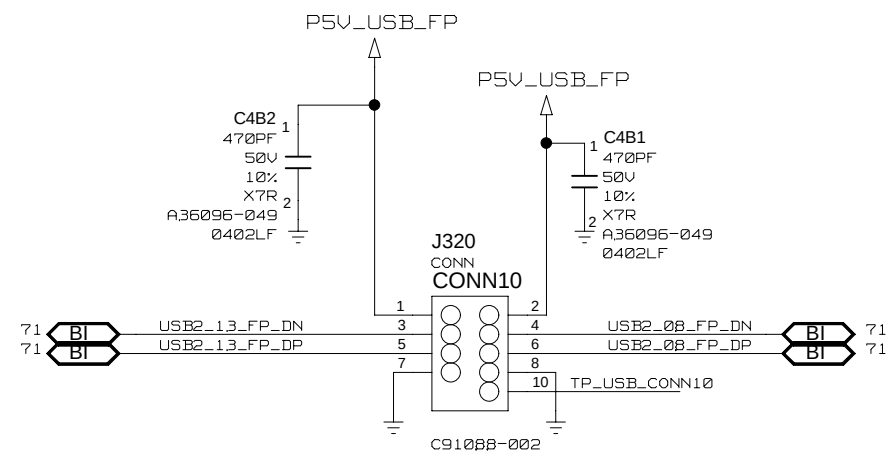
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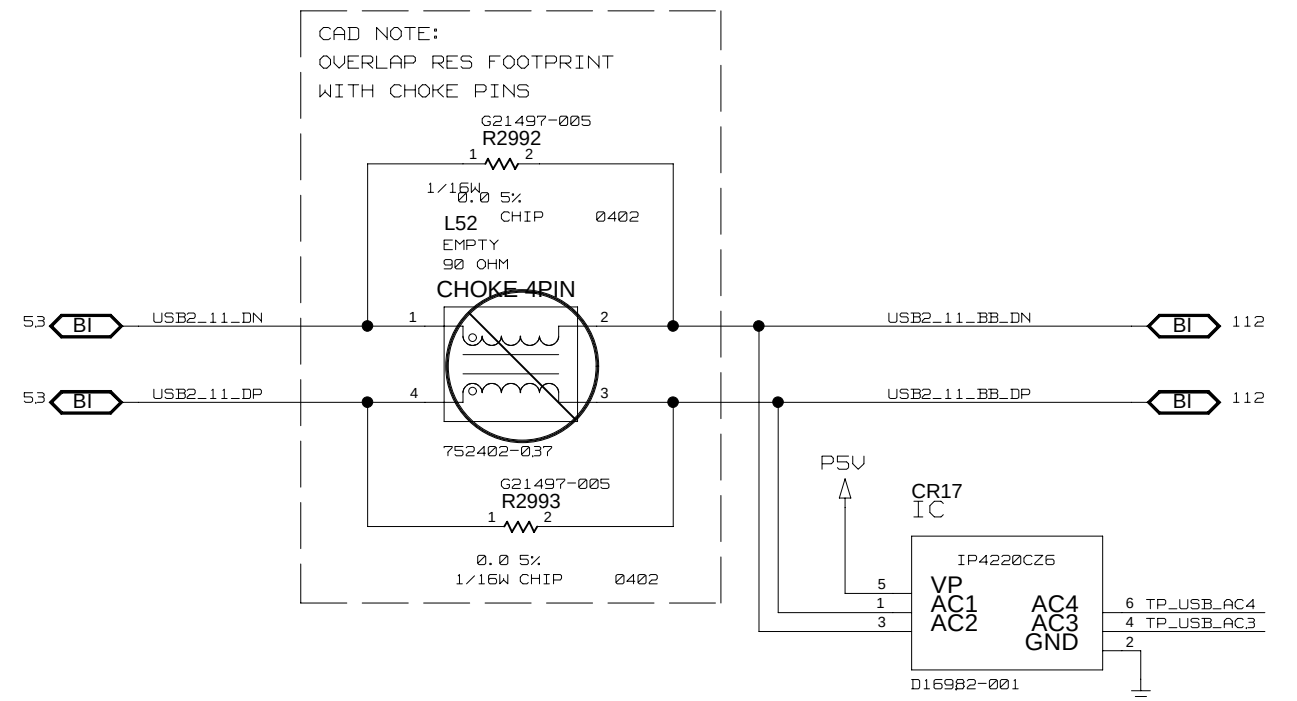
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ROOM: BRIDGE_BOARD



ROOM: FP_USB_CONN

INTERNAL USB CONN

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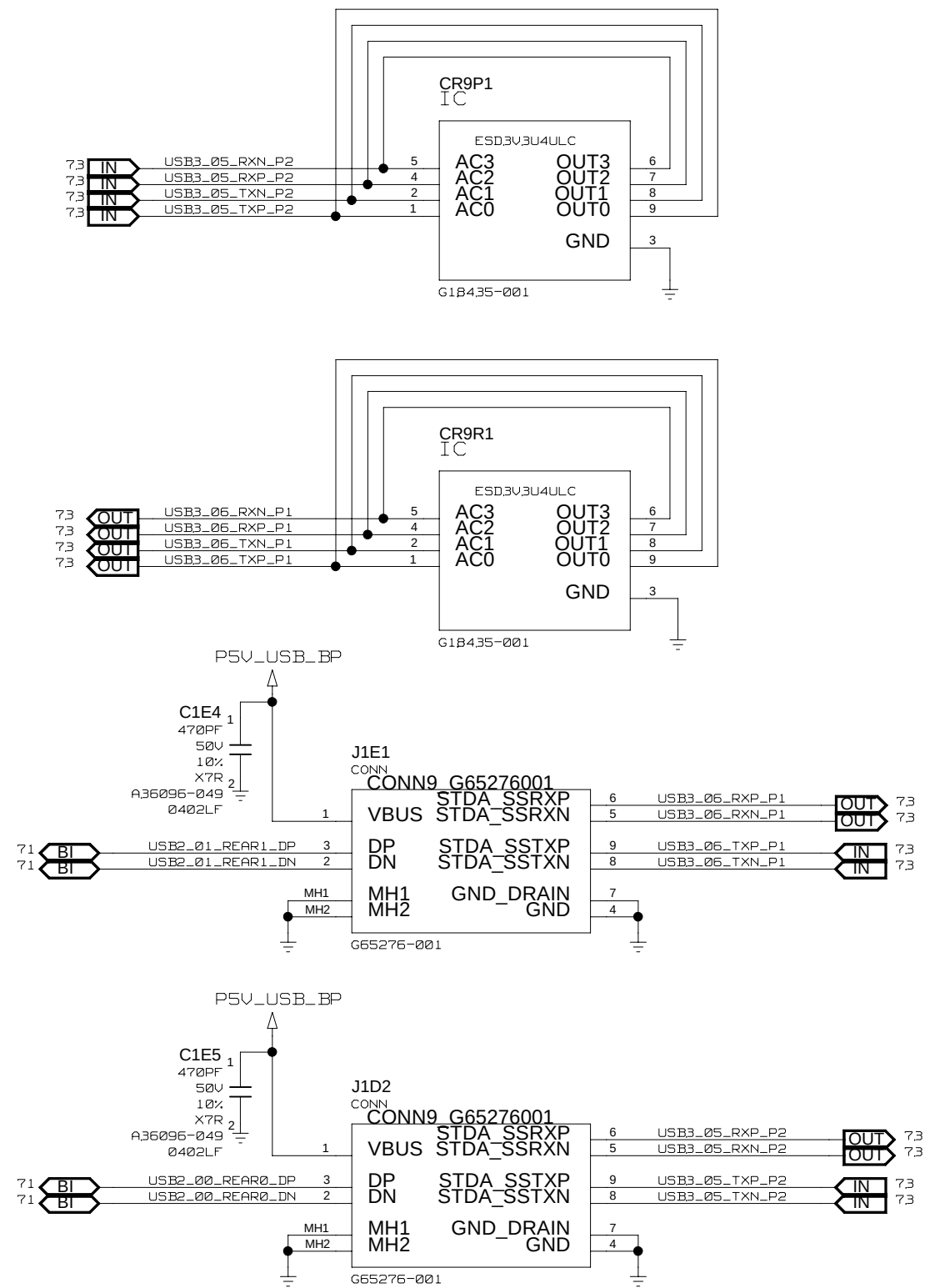
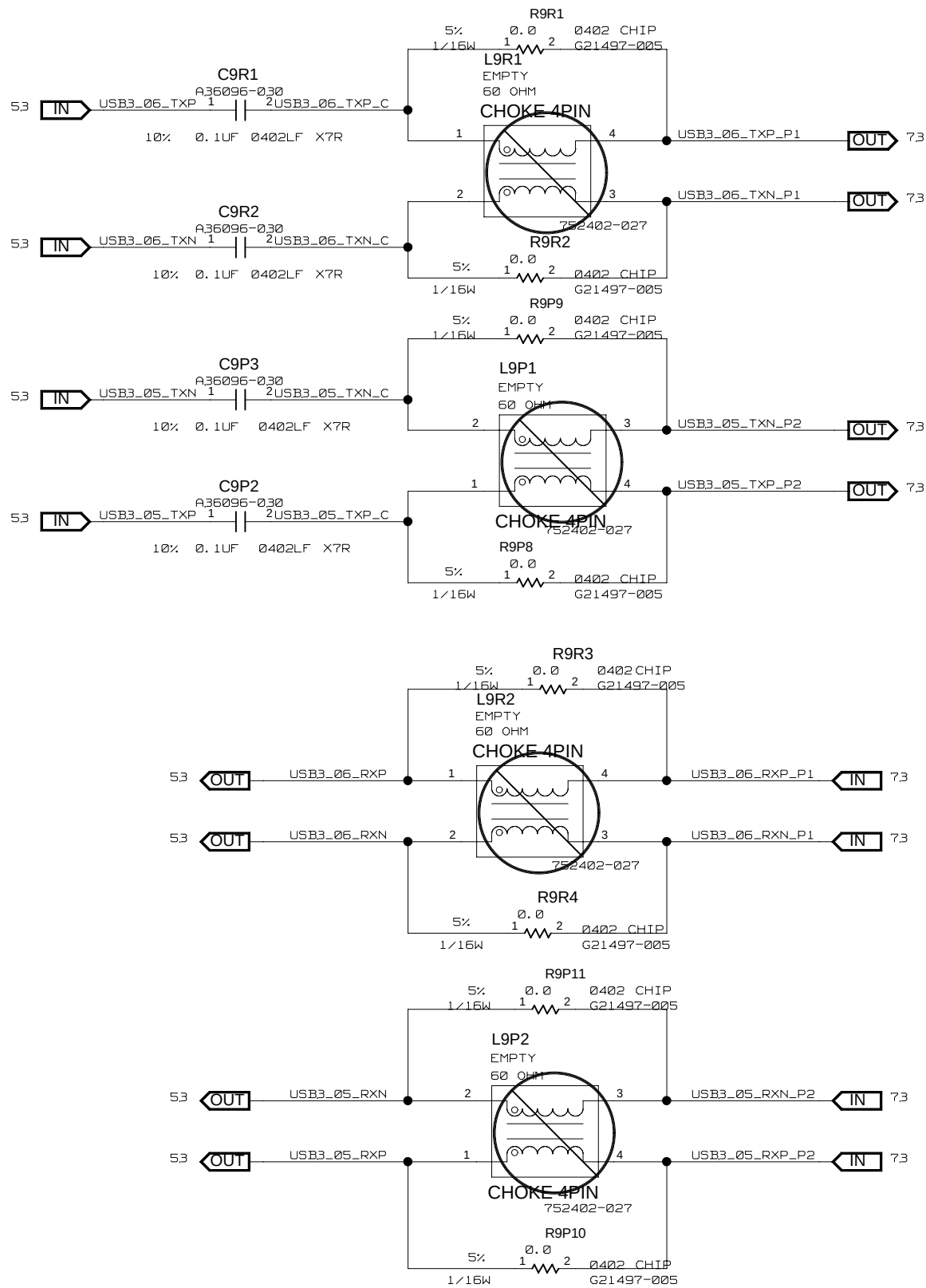
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1.3

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ROOM: BP_USB_CONN

USB3 CONN BACK PANEL

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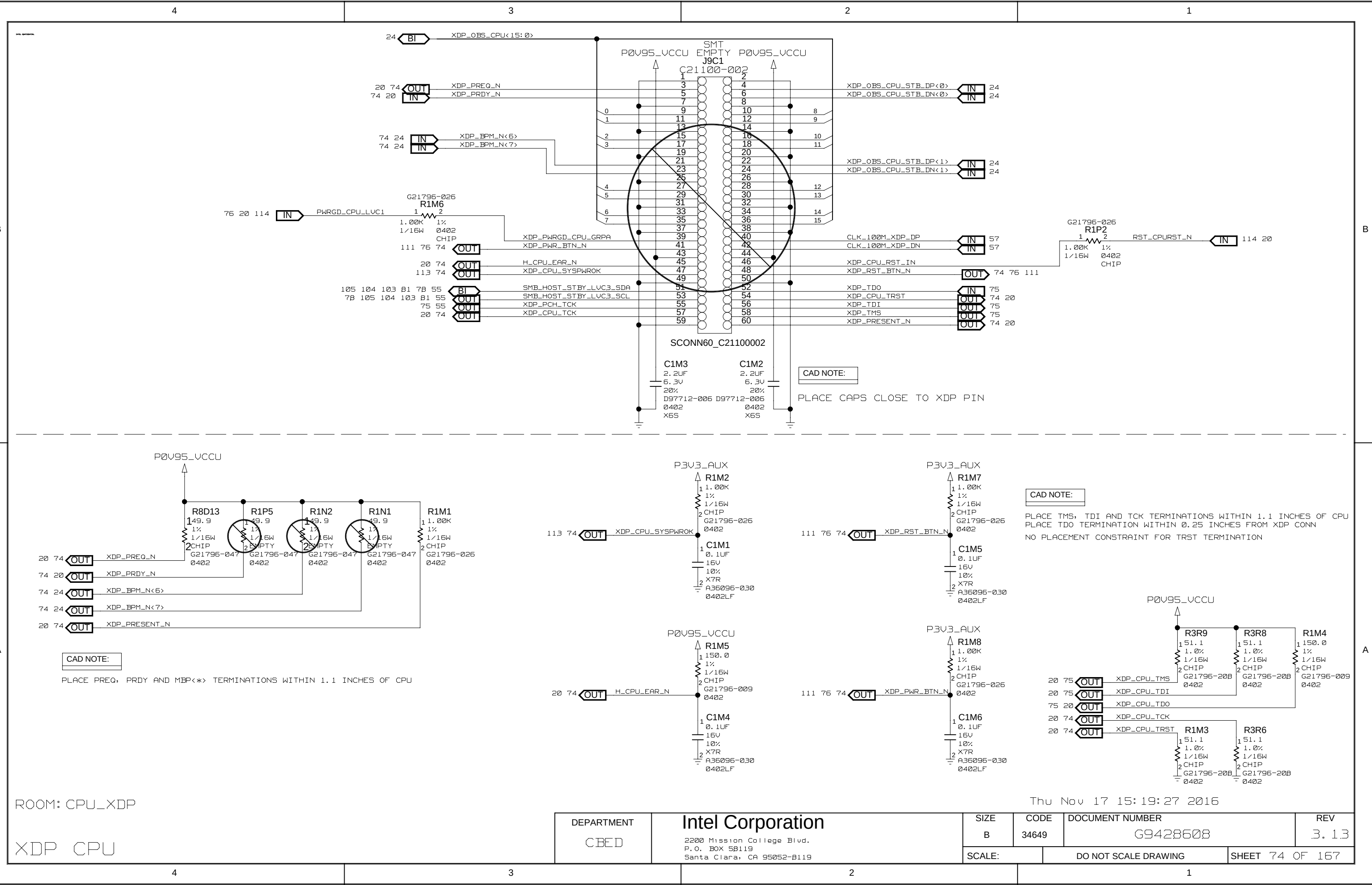
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REV
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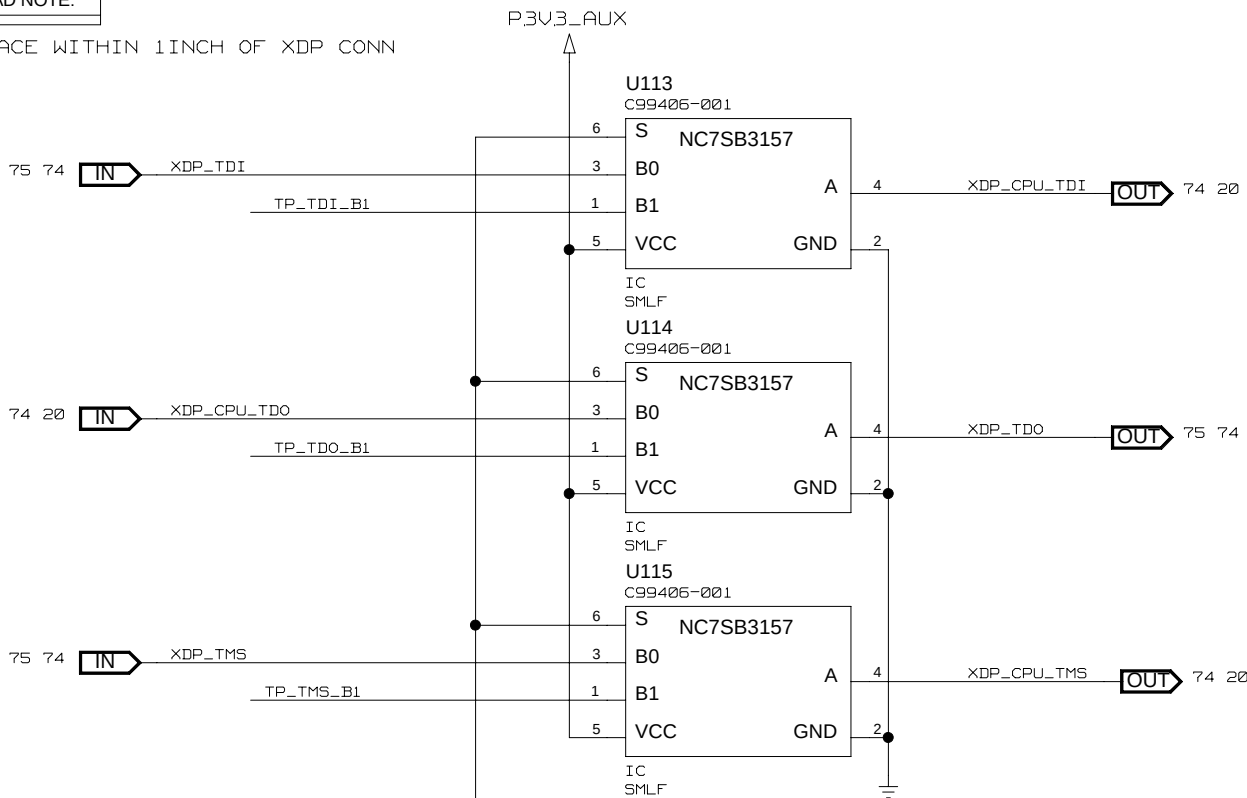
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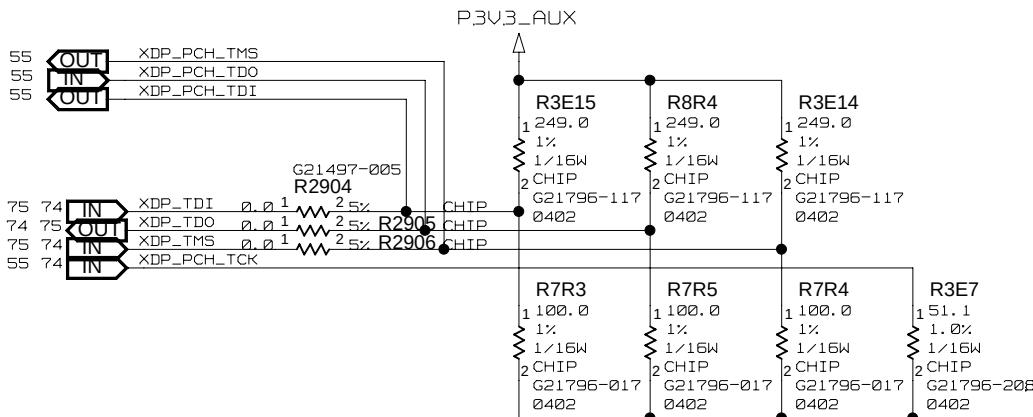


CAD NOTE:

PLACE WITHIN 1 INCH OF XDP CONN



ROOM: CPU_XDP



CAD NOTE:

PLACE TDI, TMS & TCK TERMINATIONS WITHIN 1.1 INCH FROM PCH
PLACE TDO TERMINATION WITHIN 0.25 INCHES FROM XDP CONN

ROOM: PCH_XDP

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XDP JTAG

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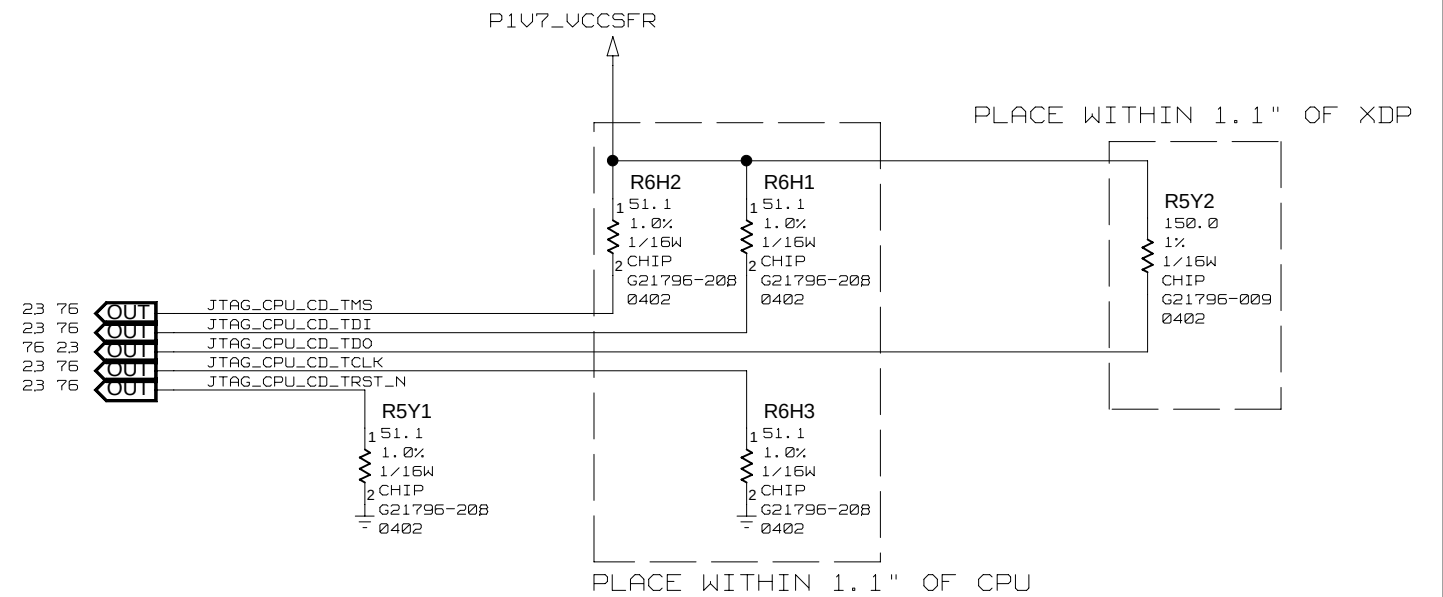
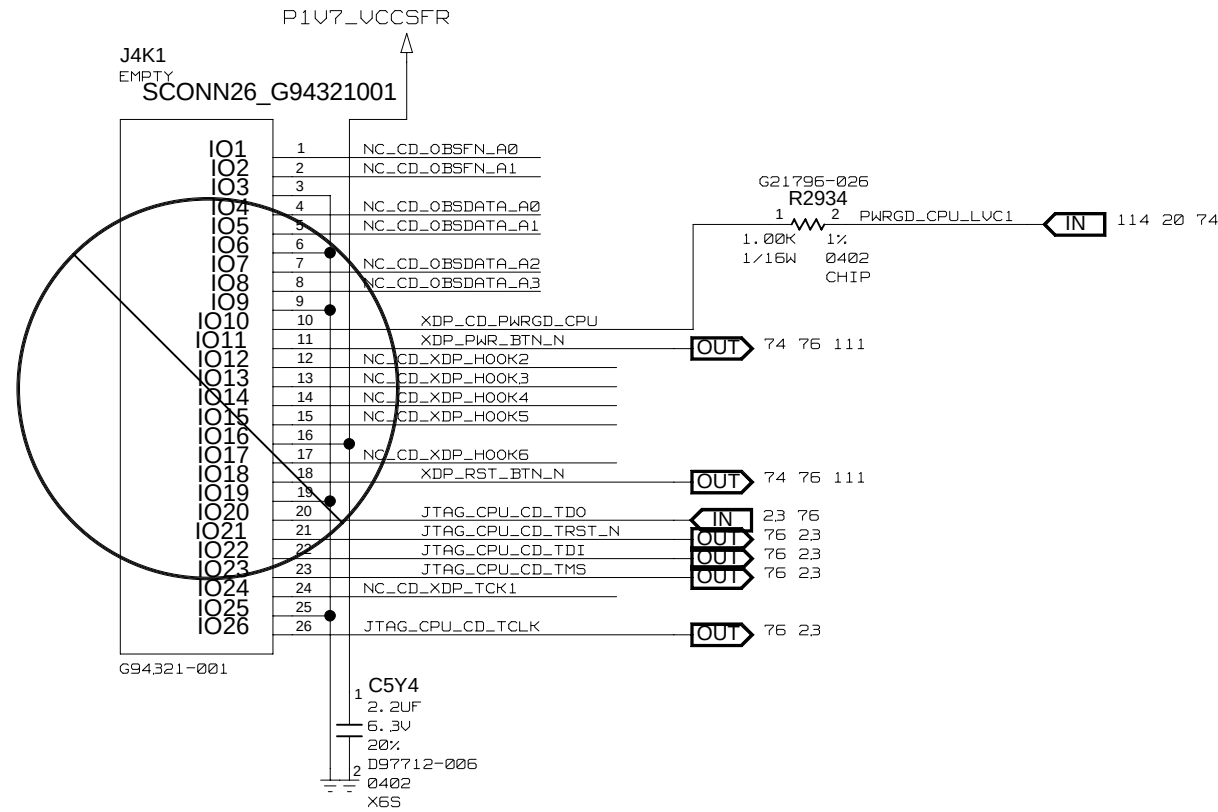
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ROOM: XDP_CD

XDP CD

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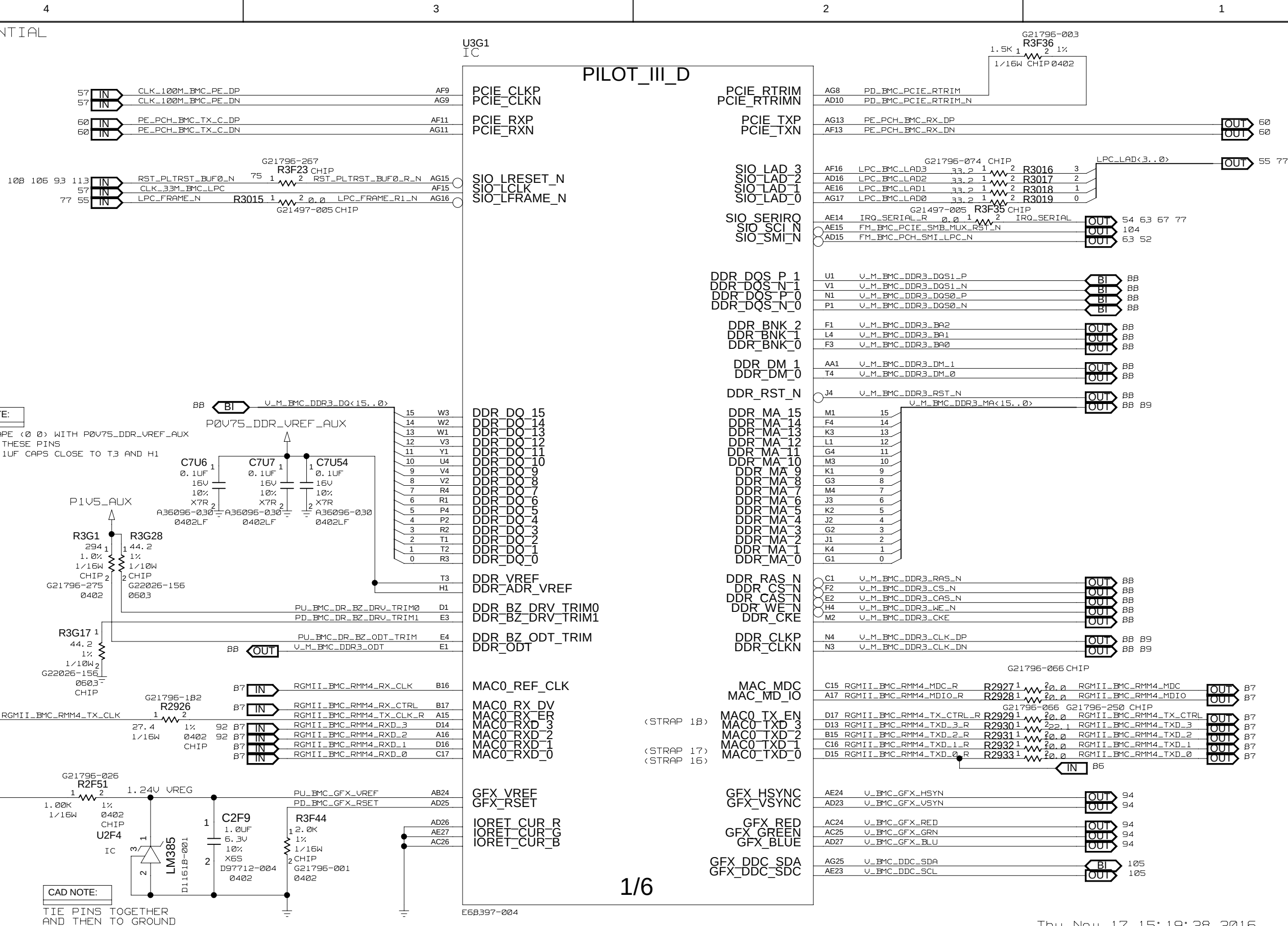
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SCALE:

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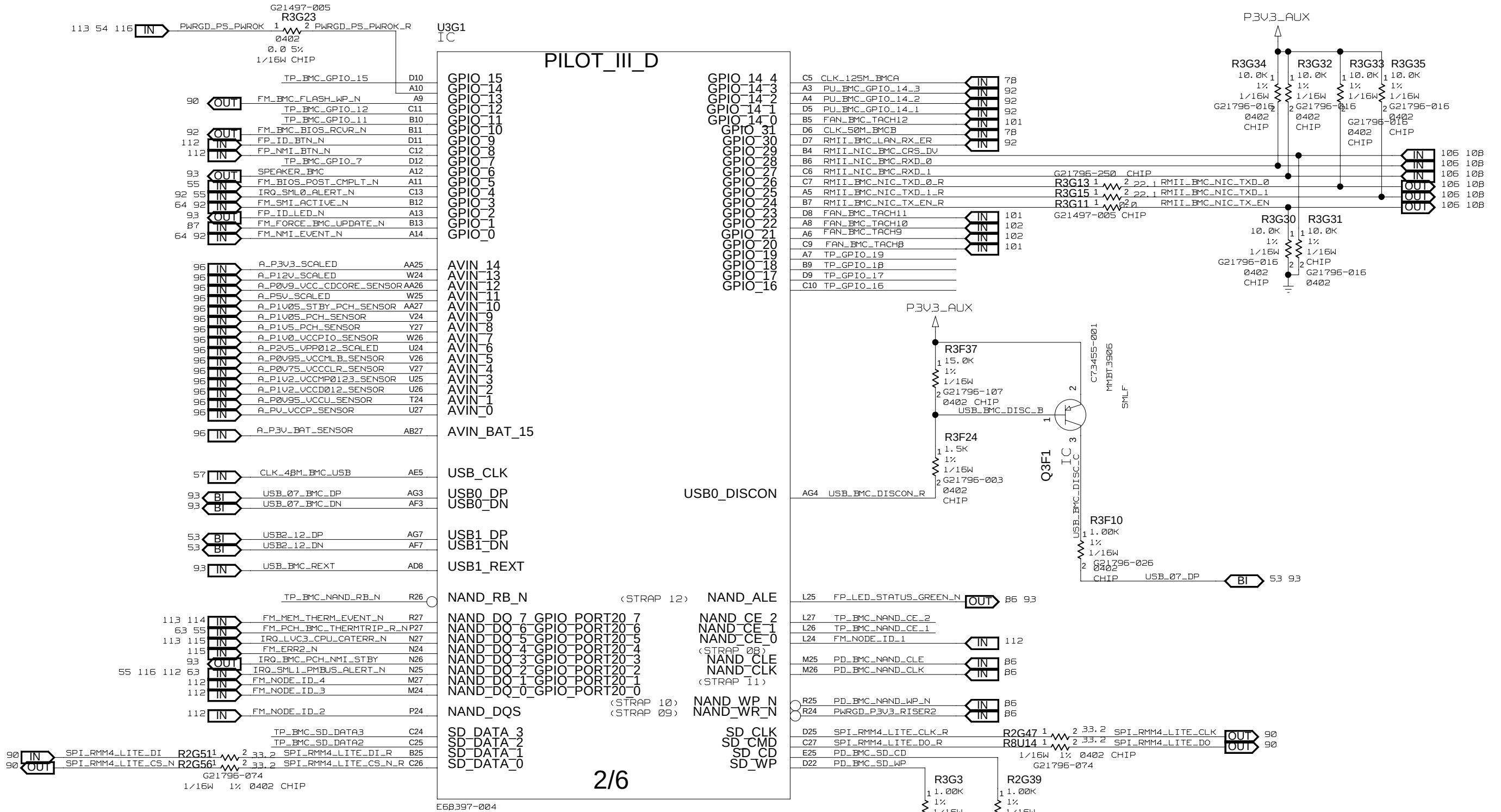
ROOM: BMC

BMC - PILOT III (1/6)

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CAD NOTE:

PLACE SERIES RESISTORS NEAR CONNECTOR

ROOM: BMC

BMC - PILOT III (2/6)

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B

B

A

A

ROOM: BMC

BMC - PILOT III (3/6)

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		SCALE:		DO NOT SCALE DRAWING	SHEET 81 OF 167	

U3G1 IC

PILOT_III_D

ADC_AVREFP
ADC_AVREFN

SDA_7
SDC_7
SDA_6
SDC_6
SDA_5
SDC_5
SDA_4
SDC_4
SDA_3
SDC_3
SDA_2
SDC_2
SDA_1
SDC_1
SDA_0
SDC_0

SGPIO_CLK
(STRAP 01) SGPIO_DOUT
(STRAP 13) SGPIO_LD

BMC_BOOT_SPI_CLK
BMC_BOOT_SPI_CS2_N
BMC_BOOT_SPI_CS1_N
BMC_BOOT_SPI_CS0_N
(STRAP 07) BMC_BOOT_SPI_DO

(STRAP 15) SIO_HOST_SPI_CLK
SIO_HOST_SPI_CS_N
(STRAP 19) SIO_HOST_SPI_DO

SIO_PWRREQ_N
SIO_ONCTL_N
SIO_PWRBTOUT_N

ICMB_TX_EN

3/6

E6B397-004

100 IN SGPIO_BMC_DIN AE19

90 IN SPI_BMC_BT_DI W4

TP_SIO_HOST_SPI_DI AC1

82 93 IN RST_RSMRST_BUF_R_N AC27
113 114 IN PWRGD_CUPWRGD_LVC3 AE7

113 55 IN FM_SLPS3_N AF17
111 55 IN FM_SLPS4_N AE17
82 IN FP_PWR_BTN_BMC_LOOP_N AF18

111 IN FM_INTRUDER_HDR_N AB25

78 IN CLK_25M_BMC_XTL AD7

TP_BMC_XT2 AF6

SGPIO_DIN

BMC_BOOT_SPI_DI

SIO_HOST_SPI_DI

VSBPWR_GD
VDDPWR_GD

SIO_SLPS3_N
SIO_SLPS5_N
SIO_PWRBTIN_N

CHASI_N

XT1_1

XT2_1

T26 TP_P2V5_BMC_AVREF

T25

F26 SMB_PMBUS_SML1_STBY_LVC3_SDA

D26 SMB_PMBUS_SML1_STBY_LVC3_SCL

G26 SMB_SENSOR_STBY_LVC3_SDA

D27 SMB_SENSOR_STBY_LVC3_SCL

F27 SMB_SML0_STBY_LVC3_SDA_R

F24 SMB_SML0_STBY_LVC3_SCL_R

G27 SMB_HSBP_STBY_LVC3_SDA

F25 SMB_HSBP_STBY_LVC3_SCL

H24 SMB_HOST_STBY_LVC3_SDA

E26 SMB_HOST_STBY_LVC3_SCL

H27 SMB_PCI_STBY_LVC3_SDA

E27 SMB_PCI_STBY_LVC3_SCL

J24 SMB_CHAS_SENSOR_STBY_LVC3_SDA

G24 SMB_CHAS_SENSOR_STBY_LVC3_SCL

J26 SMB_IPMB_STBY_LVC3_SDA

G25 SMB_IPMB_STBY_LVC3_SCL

AF21 SGPIO_BMC_CLK_R

AG21

AF19

AA2 SPI_BMC_BT_CLK_R

AA4 TP_BMC_BOOT_SPI_CS2

AA3 TP_BMC_BOOT_SPI_CS1

AB2 SPI_BMC_BT_CS_R_N

Y4 SPI_BMC_BT_DO_R

AB3 FP_LED_STATUS_AMBER_N

AC3 TP_SIO_HOST_SPI_CS_N

AC2 TP_SIO_HOST_SPI_DO

AG18

AD18 FM_PS_ON_R_N

AD17

T27 TP_BMC_BMC_TX_EN

55 103 104 112 116

55 103 104 112 116

92 97 98

92 97 98

CHIP 0.0 1

CHIP 0.0 1

92 112

92 112

55 74 78 103 104 105

55 74 103 104 105 78

92 104

92 104

92 112

92 112

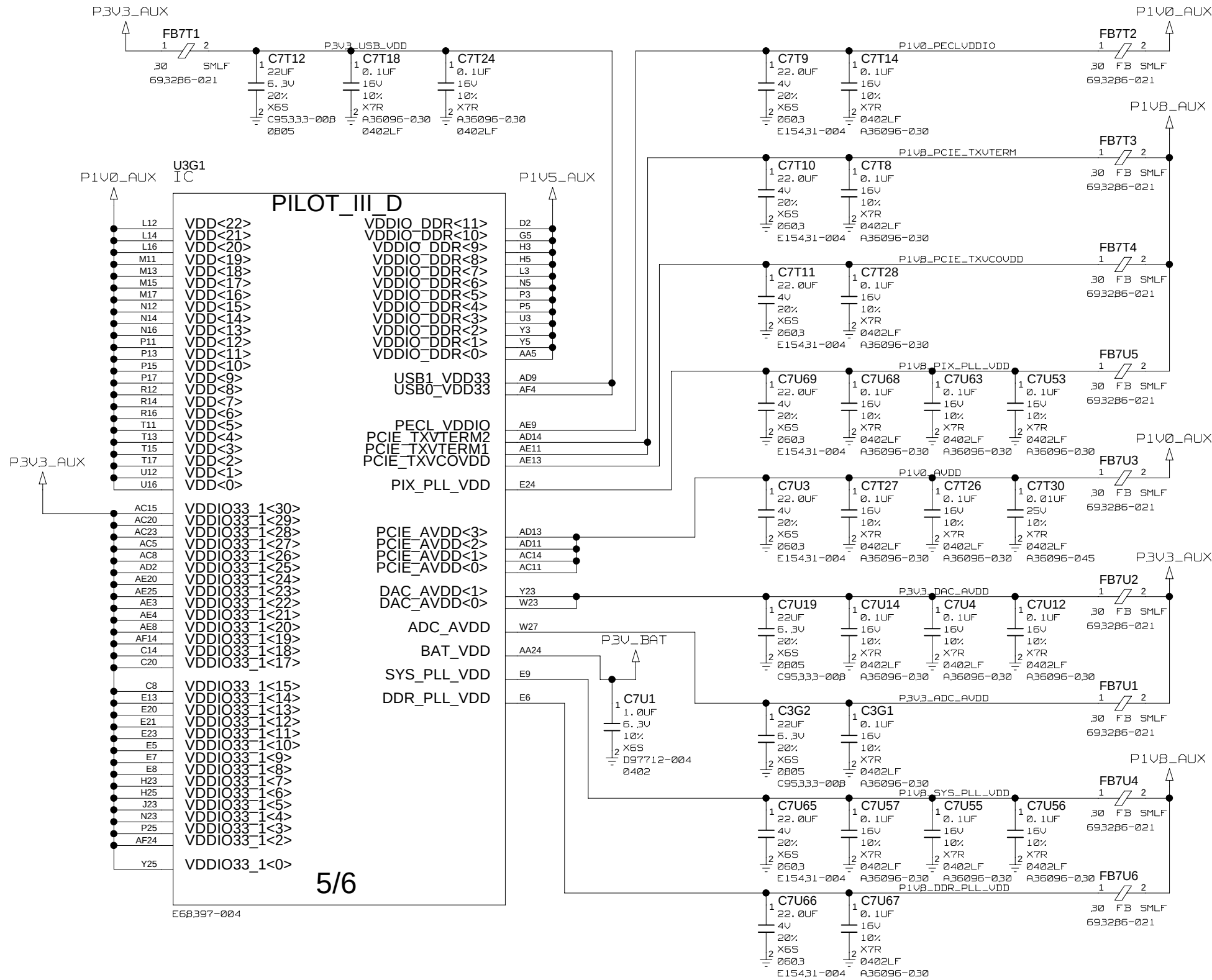
92 105

92 105



BMC - PILOT III (4/6)

1



ROOM: BMC

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BMC - PILOT III (5/6)

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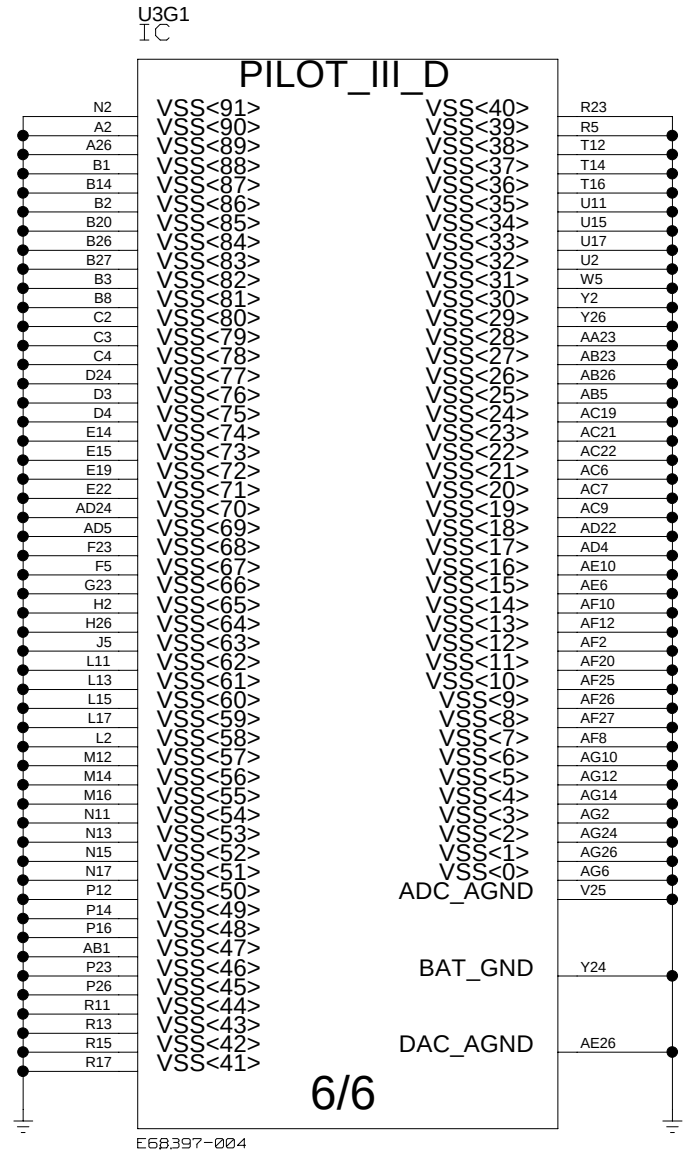
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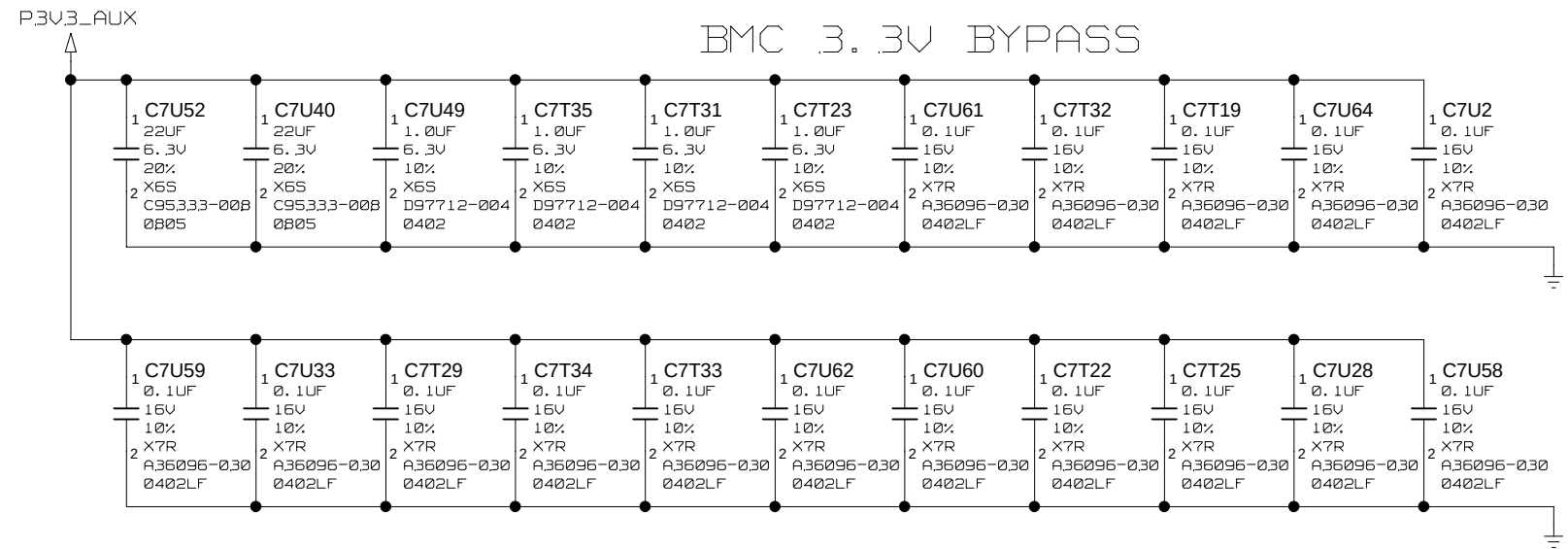
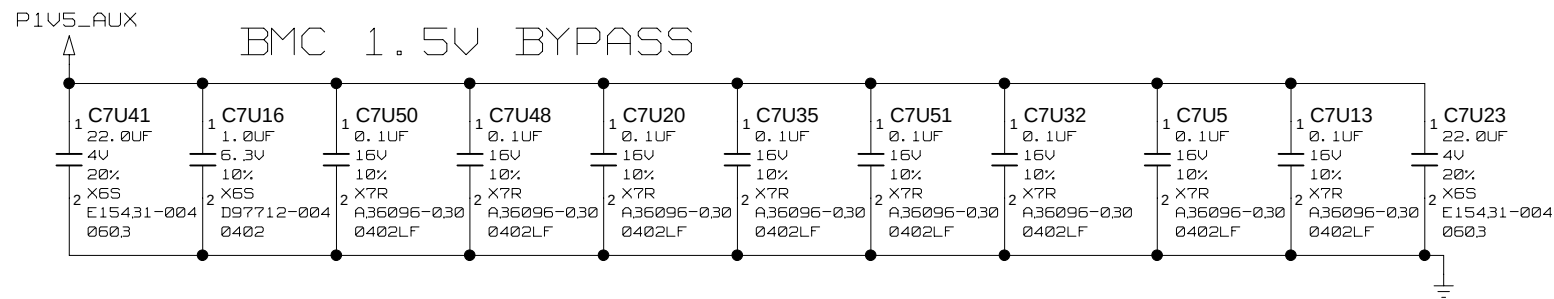
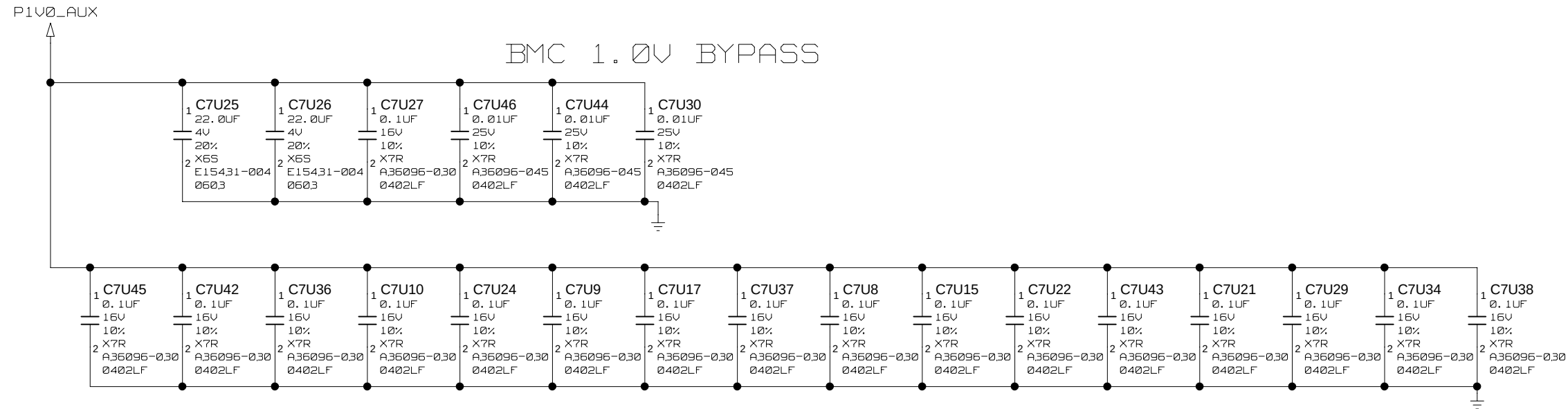
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BMC - PILOT III (6/6)

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ROOM: BMC

BMC DECOUPLING

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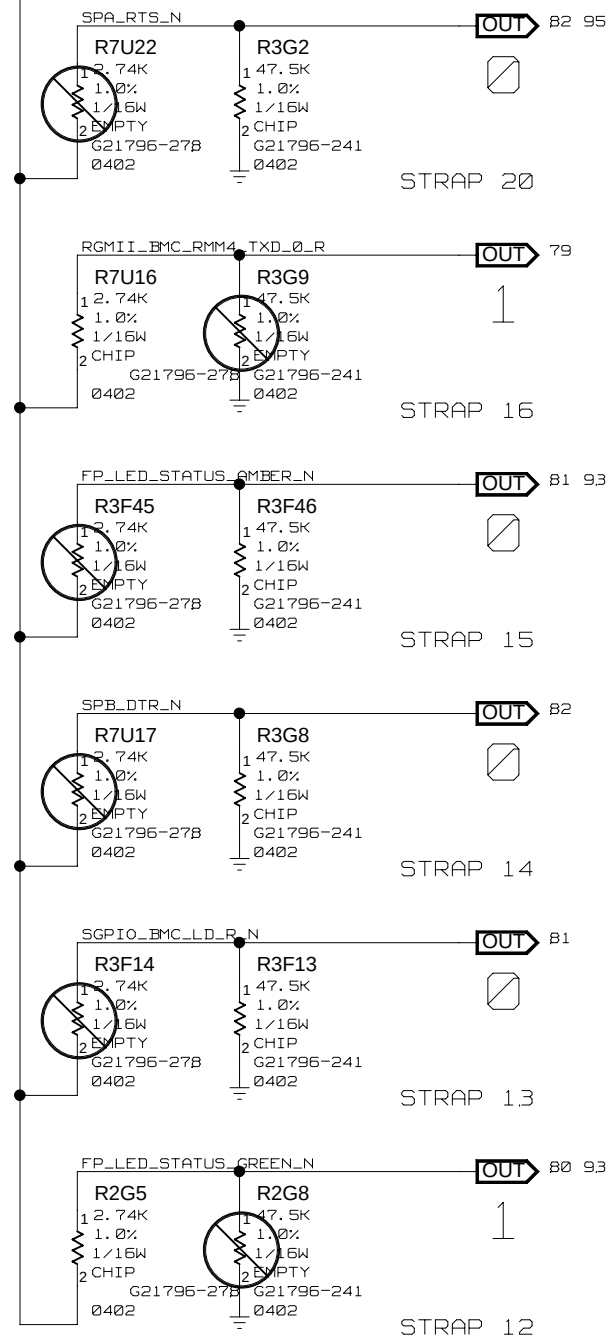
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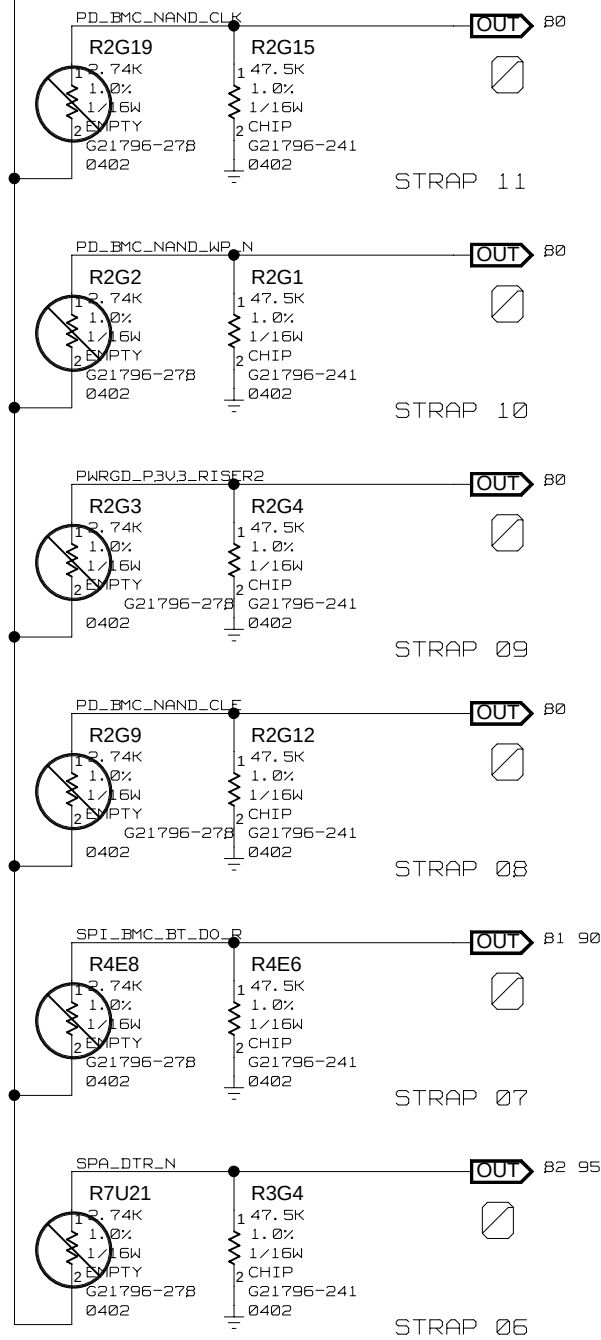
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BMC STRAP OPTIONS TABLE			
STRAP NUM	BALL NUM	BALL NAME	STRAP NAME FUNCTIONAL DISCRIPTION
20	A23	UART0_RTS_N	RGMI1_1_MODE_STRAP 0: ETHERNET PORT B IS RMII 1: ETHERNET PORT B IS RGMI1
19	AC2	SIO_HOST_SPI_DO	RESERVED
18	D17	MAC0_TX_EN	RESERVED
17	C16	MAC0_TXD_1	RESERVED
16	D15	MAC0_TXD_0	<15 0>HSPI_SWAP_SIZE_STRAP_1 & <15 0>HSPI_SWAP_SIZE_STRAP_0 DETERMINE SIZE OF SPI MEMORY ON SPI HOST PORT 00: MEM SIZE 2 MBYTES 01: MEM SIZE 4 MBYTES 10: MEM SIZE 8 MBYTES 11: MEM SIZE 16 MBYTES
15	AB3	SIO_HOST_SPI_CLK	
14	D19	UART1_DTR_N	HSPI_SWAP_EN_STRAP 0: USE DEFAULT SYSTEM BIOS IMAGE 1: USE ALTERNATE SYSTEM BIOS IMAGE
13	AF19	SGPIO_LD	HSPI_EN_STRAP 0: SIO_HOST_SPI PINS USED AS GPIOs 1: SIO_HOST_SPI INTERFACE SELECTED
12	L25	NAND_ALE	BAR_STRAP 0: LPC HOST INTERFACE ADDRESS 2EH-2FH 1: LPC HOST INTERFACE ADDRESS 4EH-4FH
11	M26	NAND_CLK	INT ACPI_STRAP 0: EXTERNAL ACPI CTRL 1: INTERNAL ACPI CTRL
10	R25	NAND_WP_N	EEPROM_STRAP 0: OPTION ROM DISABLED 1: OPTION ROM ENABLED
09	R24	NAND_WR_N	RSTBYP_STRAP THIS IS AN INTERNAL OPTION USED DURING MANUFACTURING TEST AND SHOULD BE STRAPPED WITH A PULL- DOWN RESISTOR
08	M25	NAND_CLE	SSPJTAG_STRAP 0: JTAG INTERFACE CONNECTED TO ONLY ARM PROCESSOR 1: COMBINES INTERNAL JTAG CHAIN FOR MANUFACTURING TEST
07	Y4	BMC_BOOT_SPI_DO	UART4_STRAP 0: SDA_0 & SDC_0 ARE PORT I2C_0 1: SDA_0 & SDC_0 ARE PORT UART4
06	C22	UART0_DTR_N	SDCARD_STRAP 0: SD/MMC CARD INTERFACE NOT USED. THE PINS ARE GPIO 1: SD/MMC CARD INTERFACE ENABLED
05	A20	UART1_RTS_N	EXT_BUS_STRAP 0: NAND/EXTERNAL BUS INTERFACE NOT USED, PINS ARE GPIO 1: NAND/EXTERNAL BUS INTERFACE IS USED
04	AG19	UART3_TXD	RGMI1_0_MODE_STRAP 0: ETHERNET PORT A IS RMII 1: ETHERNET PORT A IS RGMI1
03	A21	UART2_TXD	MAC1_STRAP CONFIGURE THE ETHERNET PORT B AS GPIO<31:24> PINS 0: THESE PINS ARE USED AS GPIO<31:24> PINS 1: ETHERNET PORT B INTERFACE CONFIGURED FOR RMII RGMI1_1_MODE_STRAP, MAC1_STRAP 0 0 PINS USED AS GPIOs 0 1 PINS USED AS RMII AND THE ADDITIONAL PINS ARE GPIOs 1 0 ALL MAC1 PINS AND ADDITIONAL PINS ARE USED AS RGMI1 1 1 ALL MAC1 PINS AND ADDITIONAL PINS ARE USED AS RGMI1
02	D20	UART0_TXD	RESERVED
01	AG21	SGPIO_DOUT	ROM_BOOT_STRAP 0: BOOT FROM BMC BOOT SPI INTERFACE 1: BOOT FROM INTERNAL ROM<SCRATCHPAD REGISTERS>
00	B19	UART1_TXD	DDR2_STRAP 0: DDR3 DEVICE CONNECTED TO DDR PINS 1: DDR2 DEVICE CONNECTED TO DDR PINS

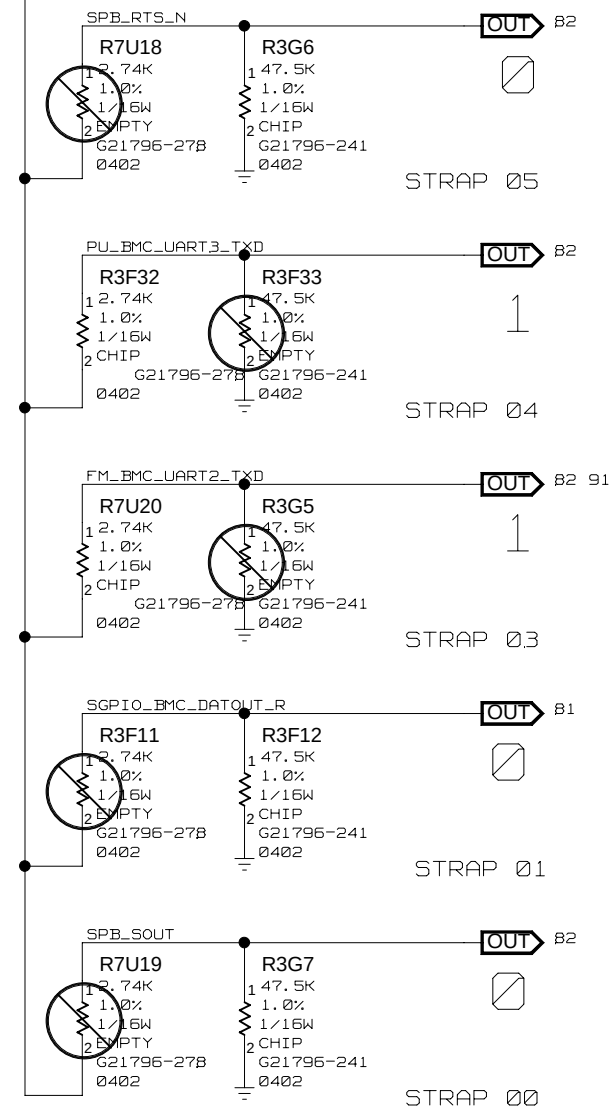
P3V3_AUX



P3V3_AUX



P3V3_AUX



BMC POWER ON RESET STRAP JUMPERS
PULL DOWN = 0 FOR OPTION
PULL UP = 1 FOR OPTION

ROOM: BMC

BMC CONFIGURATION

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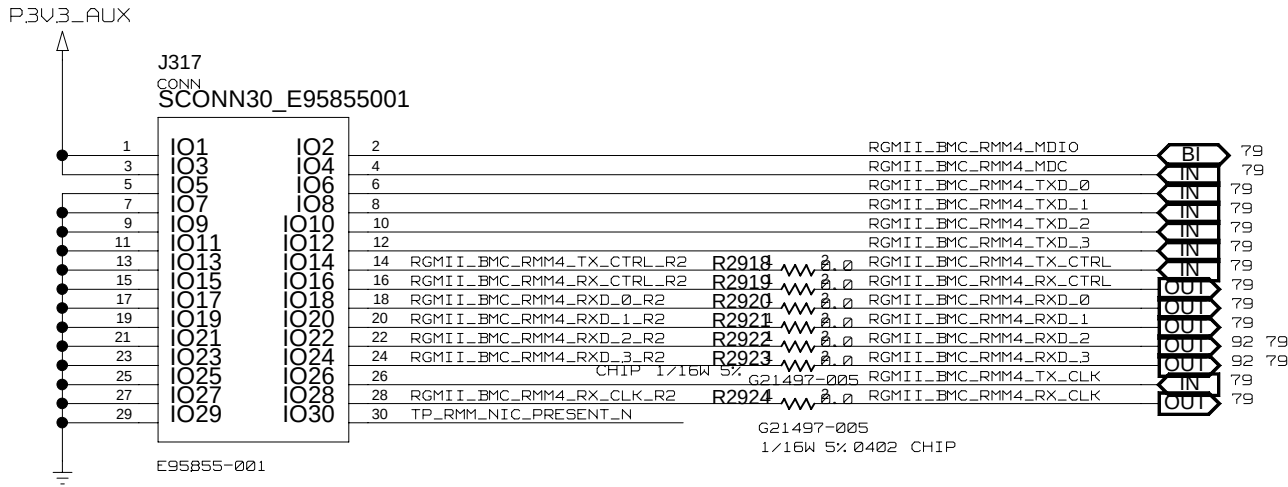
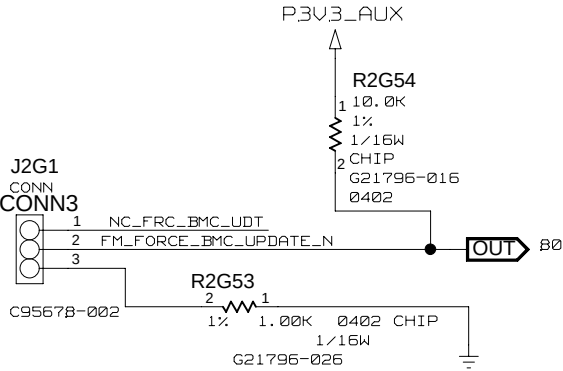
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FORCE BMC UPDATE JUMPER		
JUMPER POSITION	SIGNAL STATE	OPERATION MODE
1-2	PULLED HIGH	NORMAL
2-3	PULLED DOWN	UPDATE



ROOM: BMC

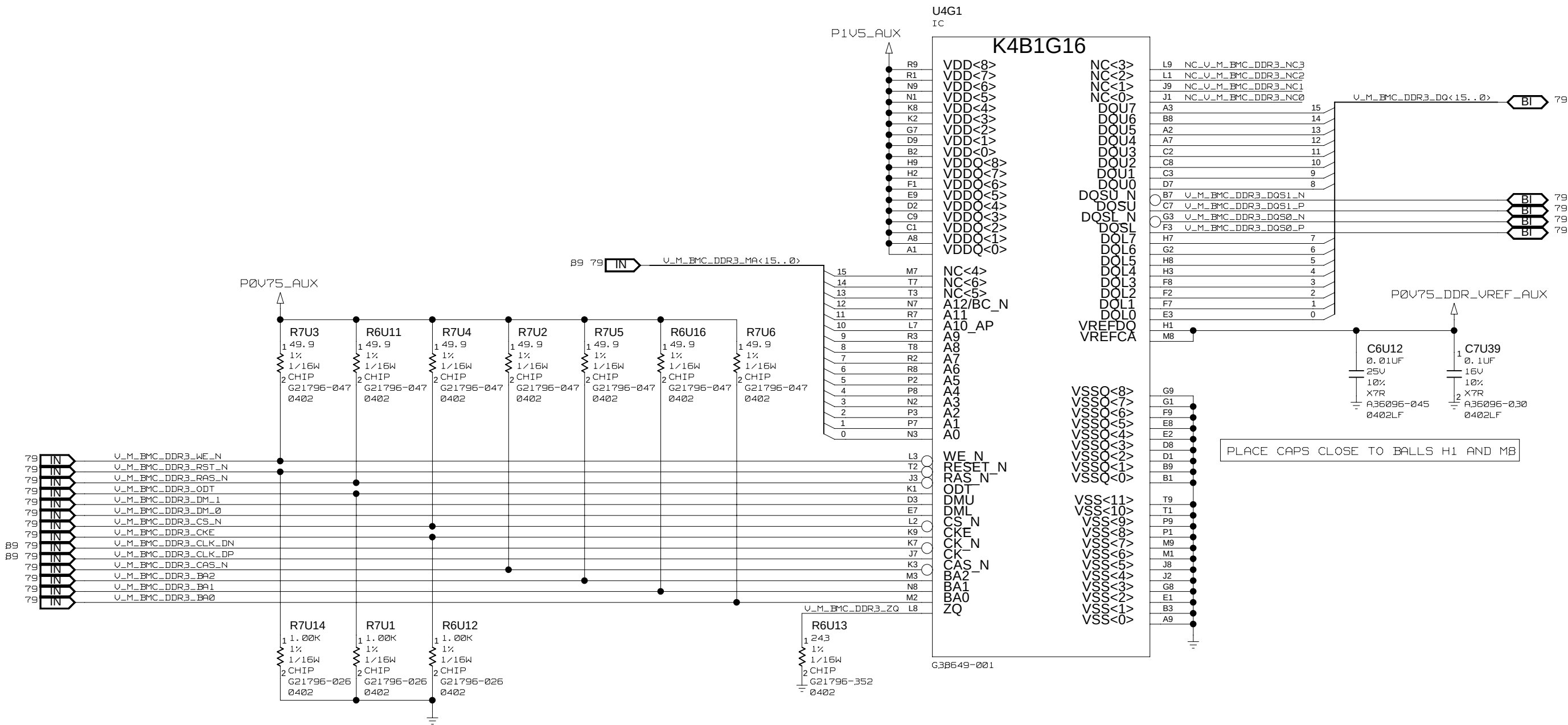
RGMII

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		SCALE:	DO NOT SCALE DRAWING		SHEET 87 OF 167

BOM NOTE:

REPLACE G38649-001 WITH H56296-001

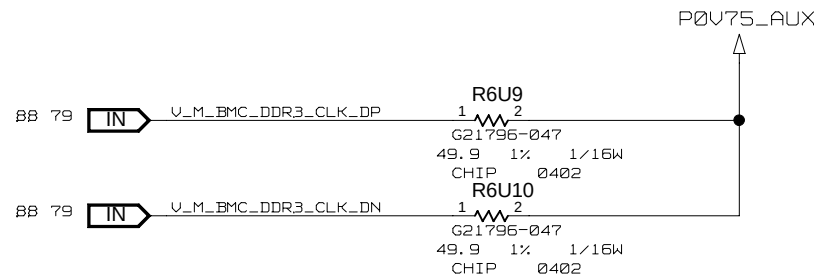
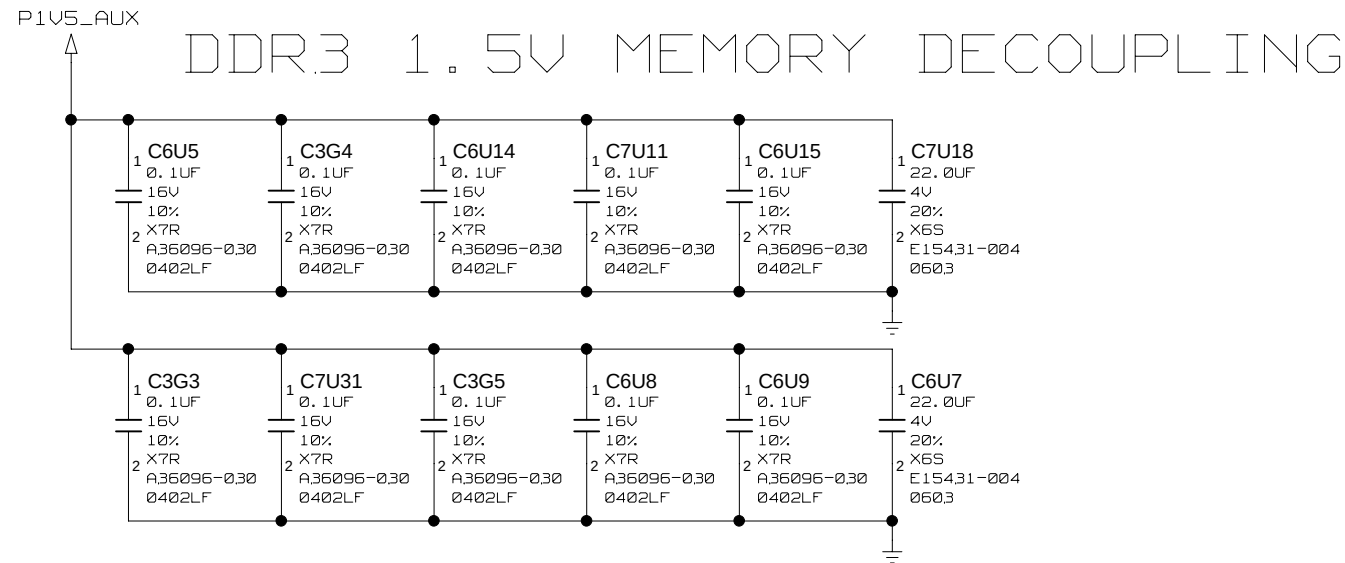
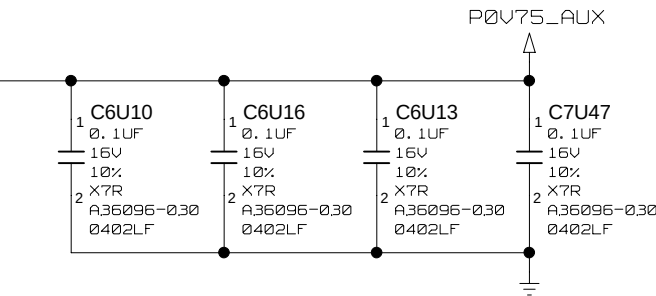
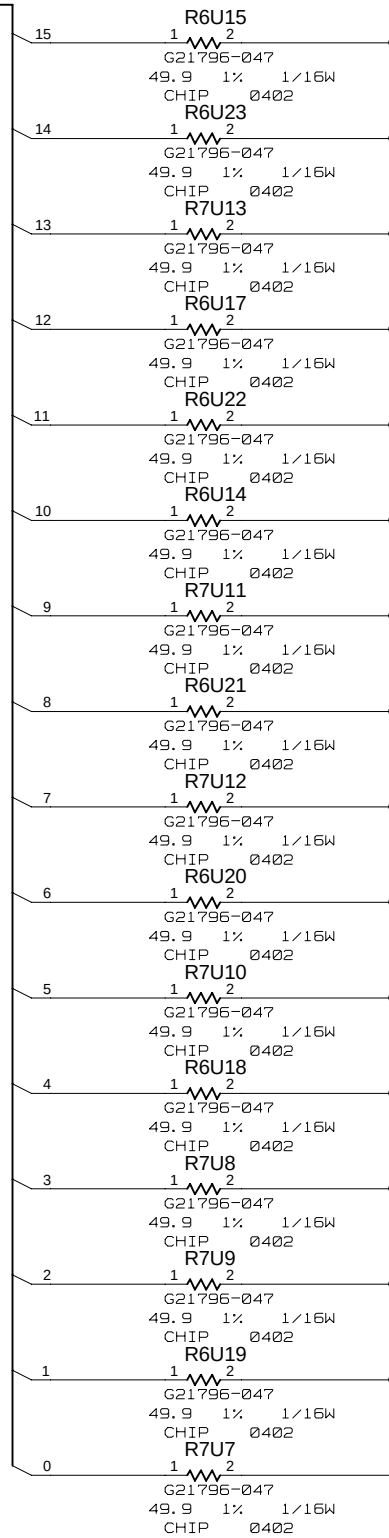


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RTAD

BB 79 IN U_M_BMC_DDR3_MA<15..0>

CAD NOTE:
PLACE RTAD RESISTORS
CLOSE TO DDR3 MEMORY
BETWEEN : 100MILS
AND 500MILS



ROOM: BMC_DDR

BMC DDR3 MEMORY

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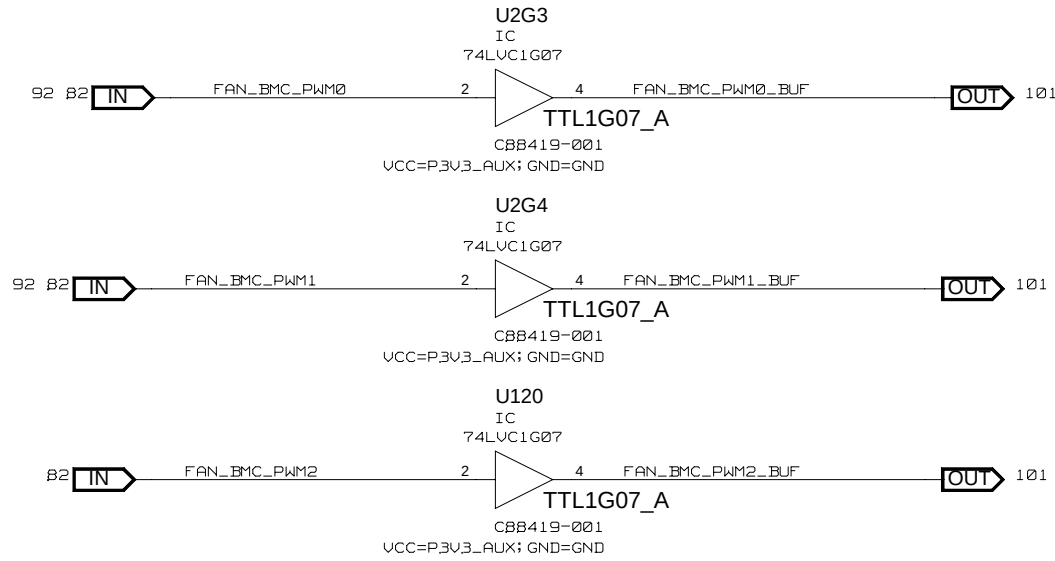
B



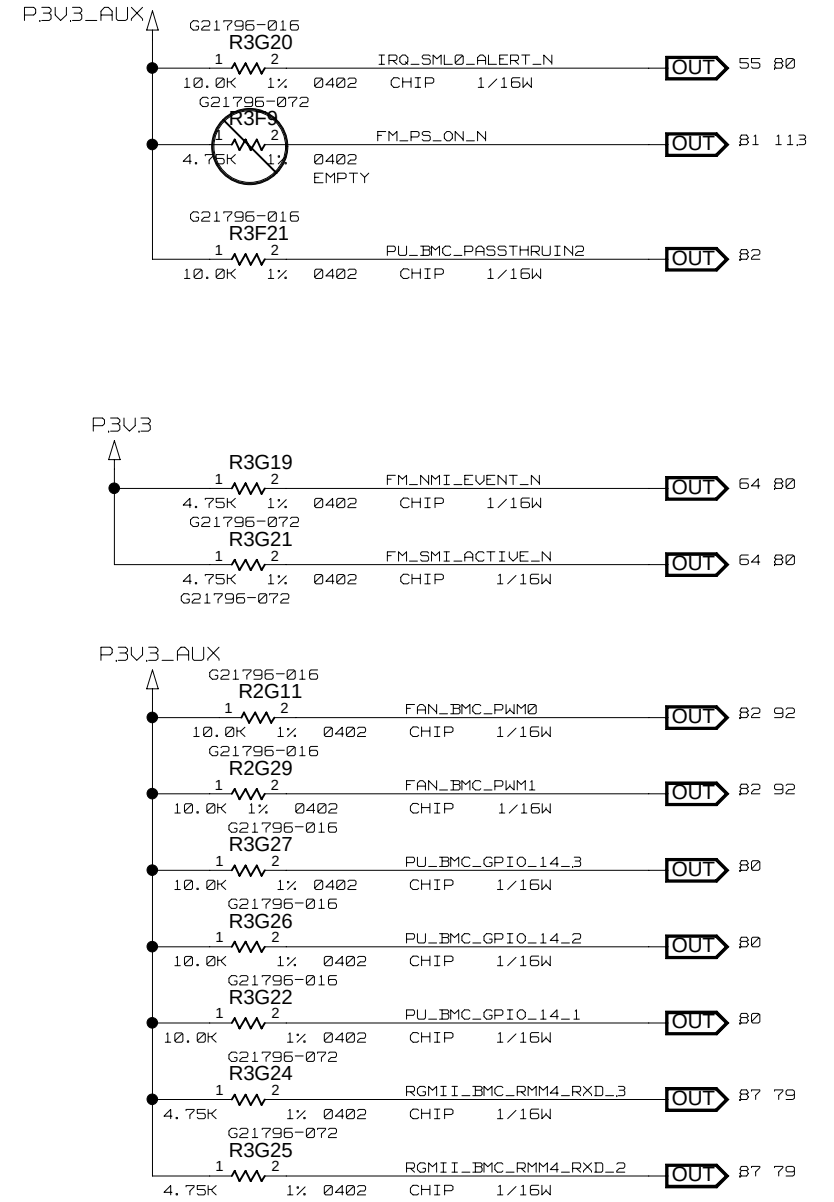
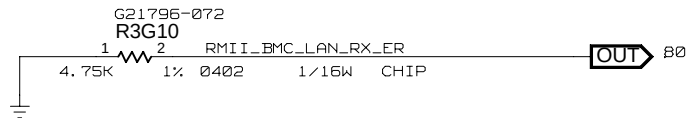
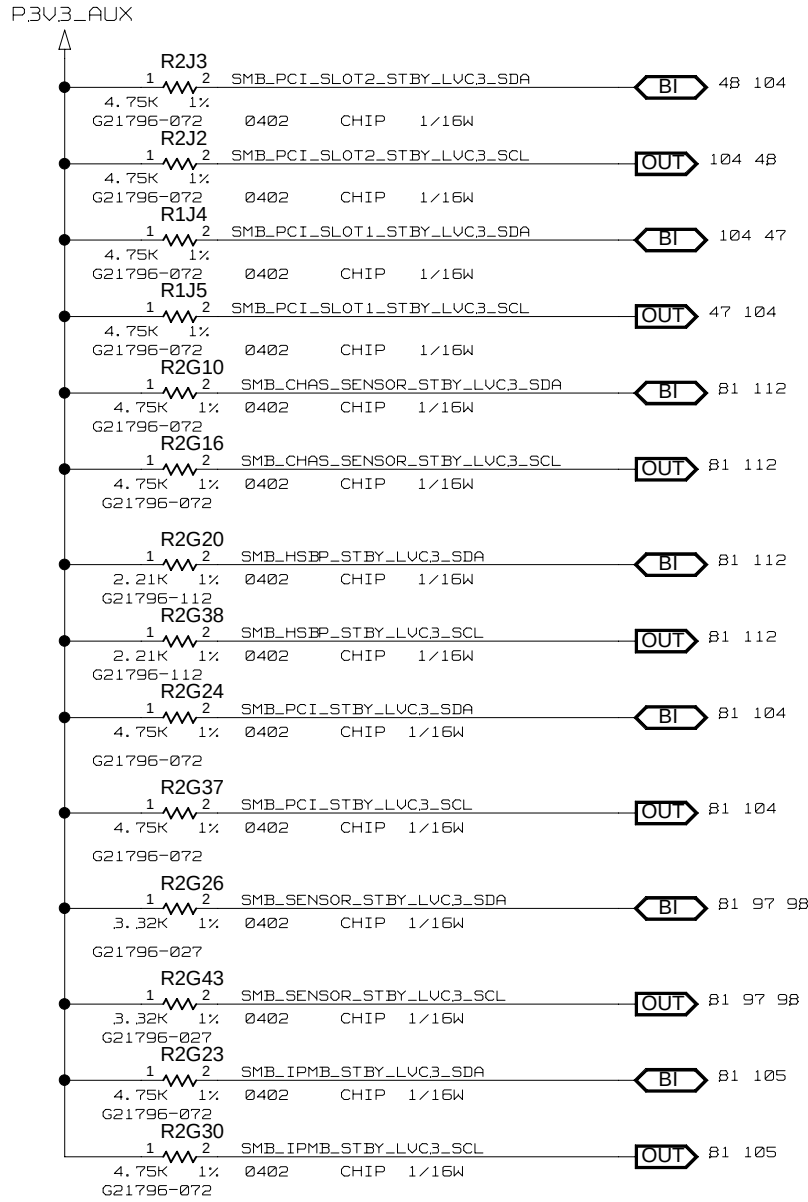
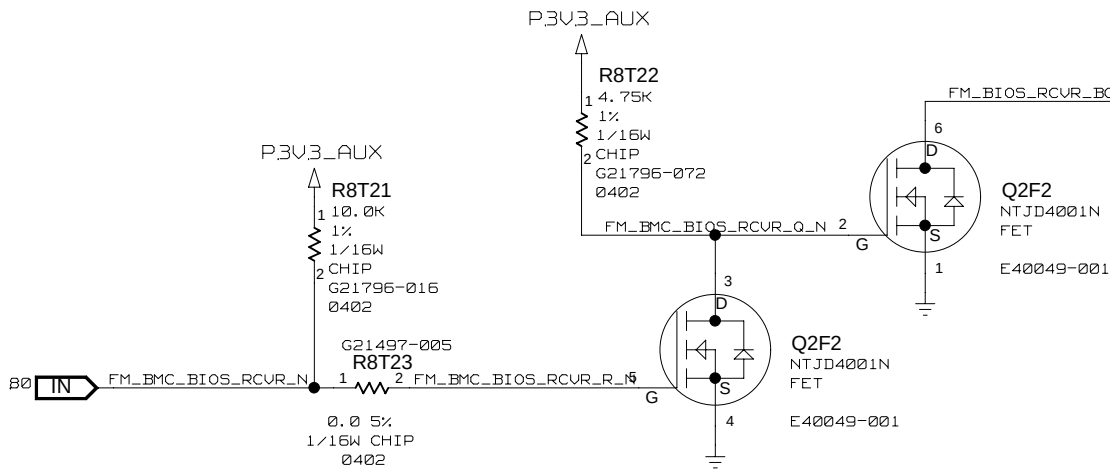
A

1

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PUT THIS BUFFER AROUND BMC



ROOM: BMC

BMC MISC

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CODE
34649

DOCUMENT NUMBER
G9428608

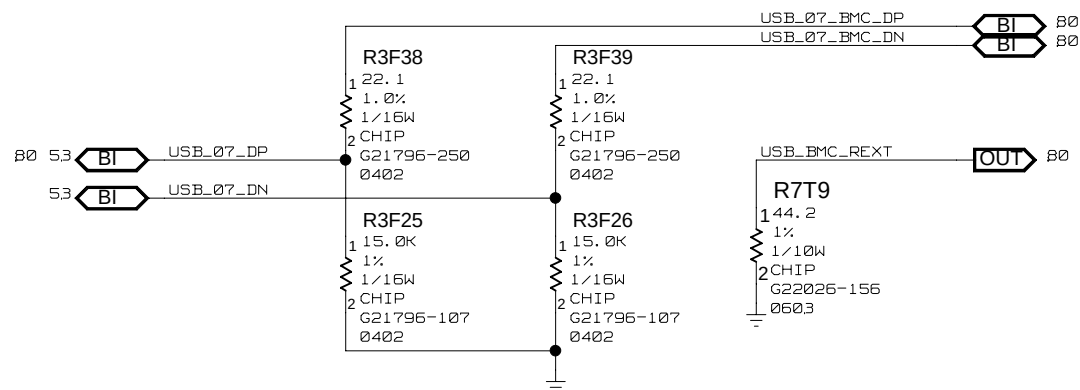
REV
3.13

SCALE:

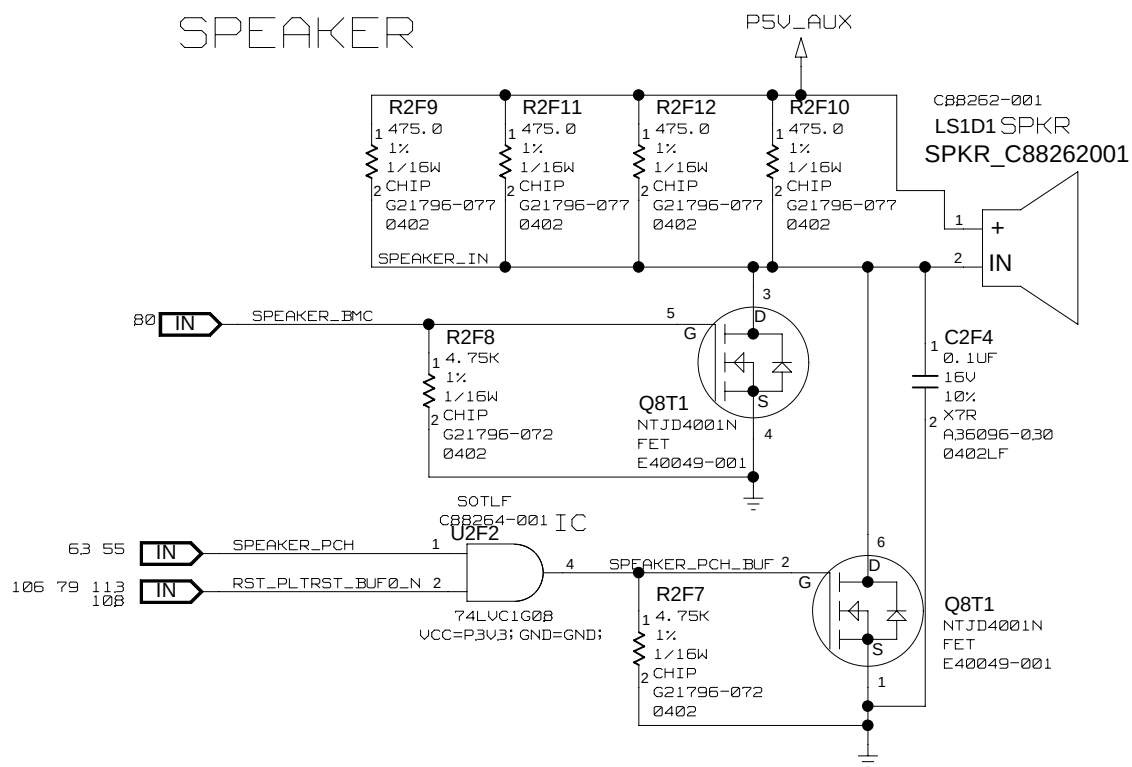
DO NOT SCALE DRAWING

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USB TERMINATIONS

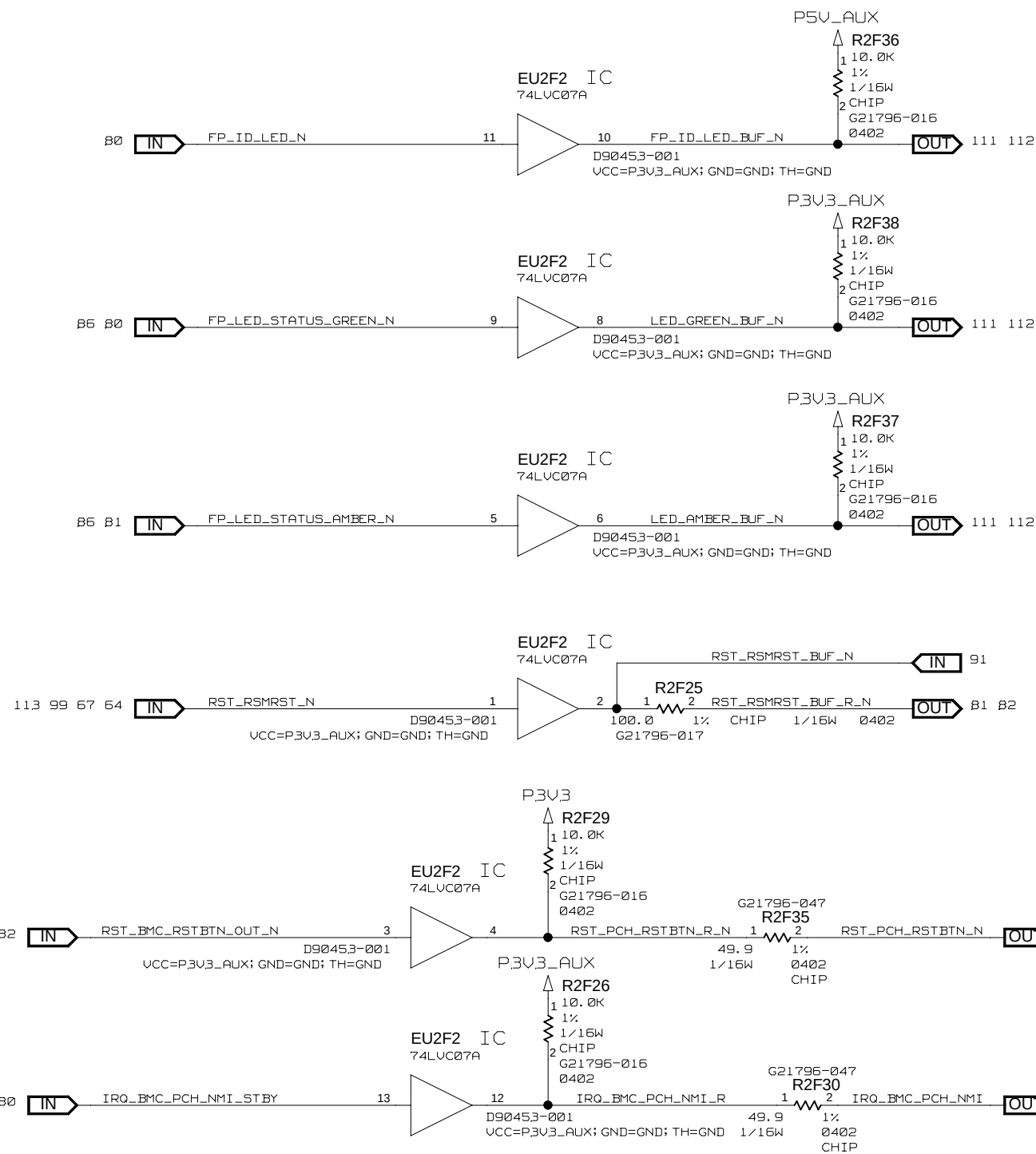


SPEAKER



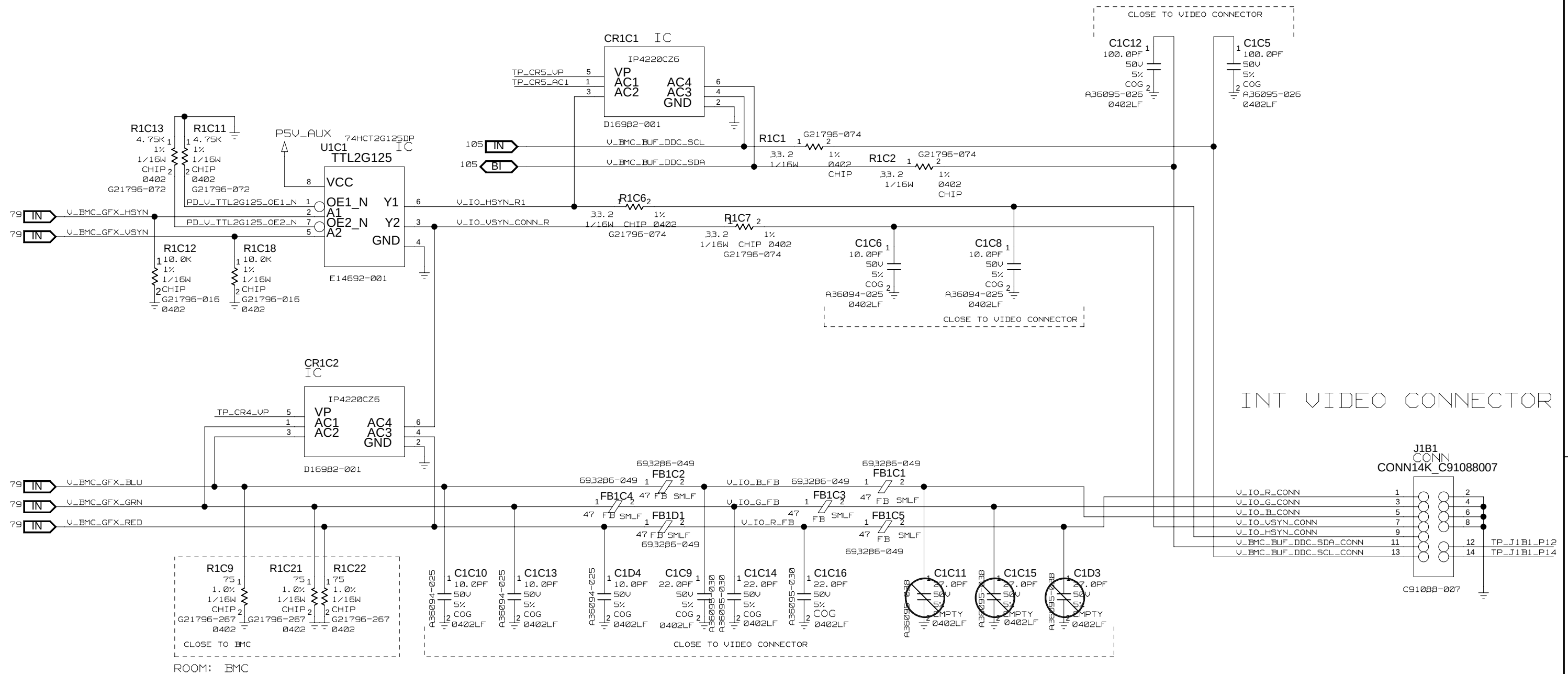
ROOM: BMC

BMC SPKR/USB



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		SCALE:	DO NOT SCALE DRAWING		SHEET 93 OF 167

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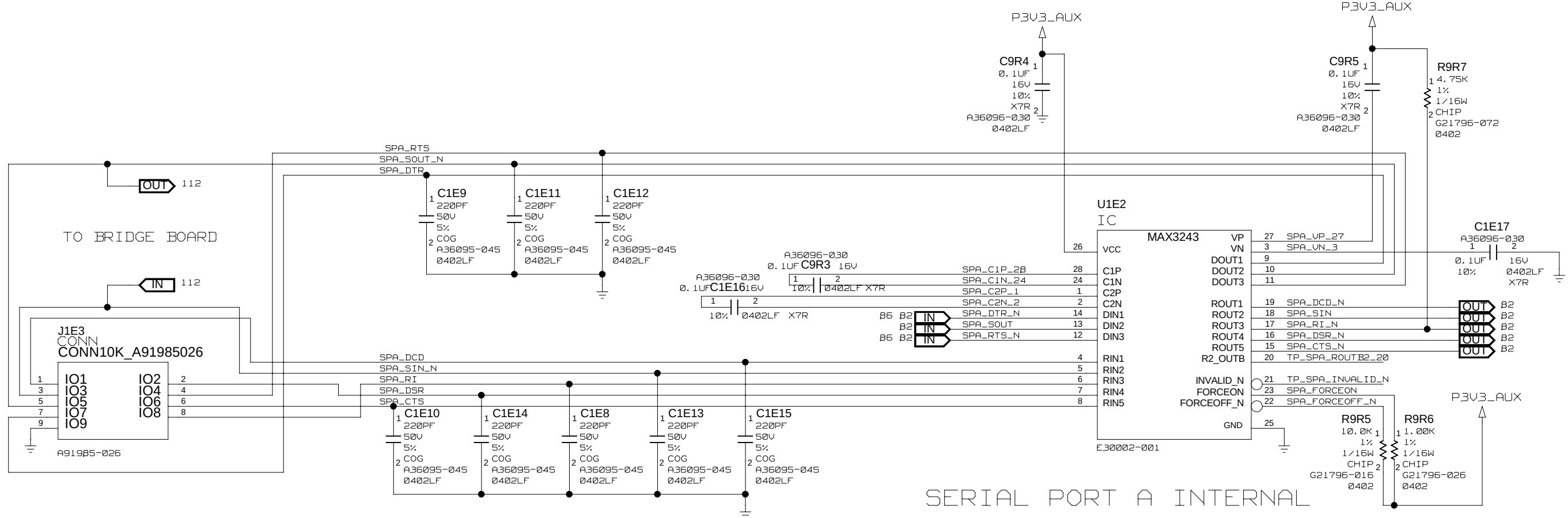
ROOM: BMC_VIDEO

BMC VIDEO

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SERIAL PORT A INTERNAL

ROOM: BMC_SERIAL

BMC SERIAL PORT

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DOCUMENT NUMBER

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REV

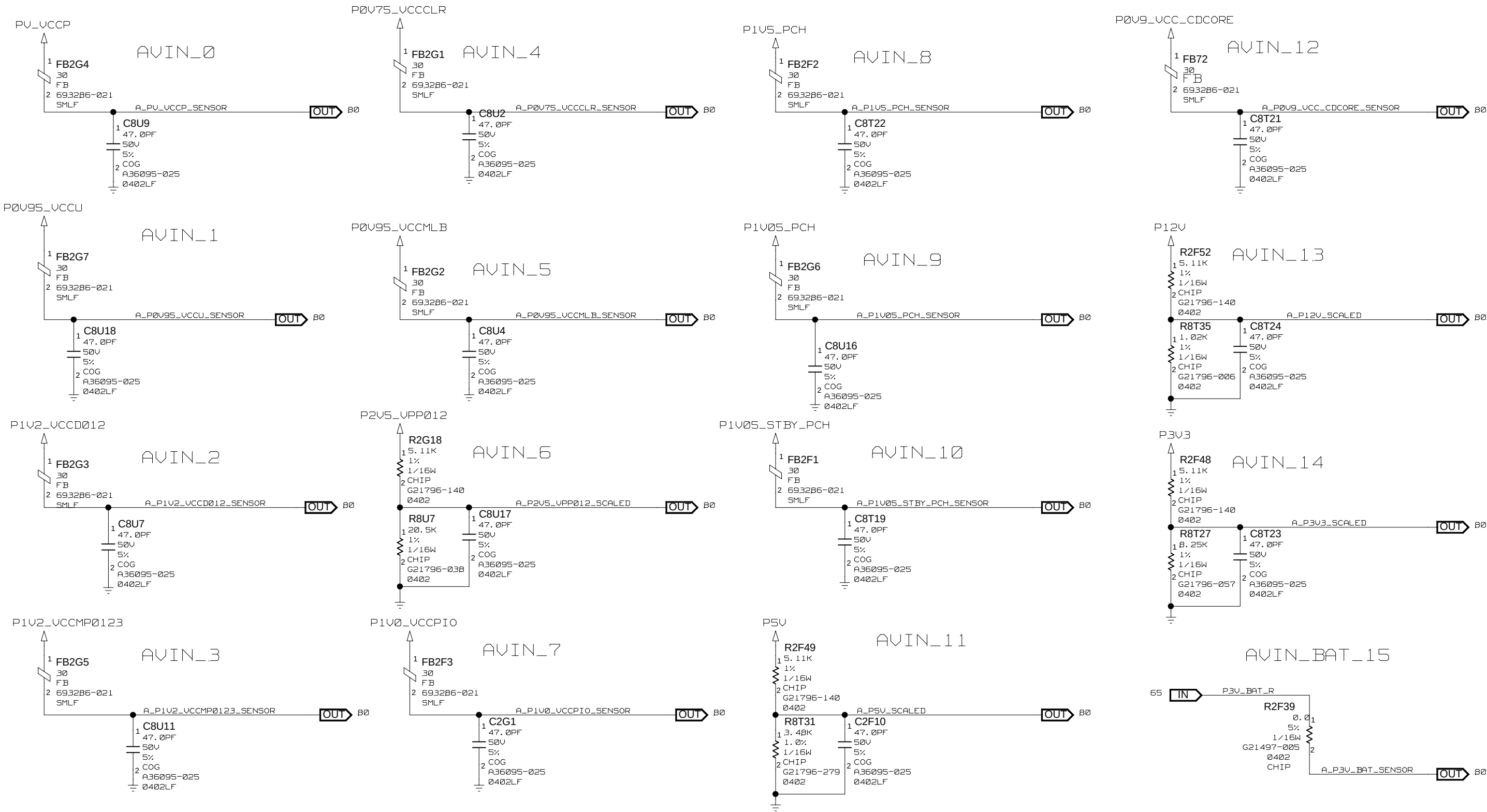
3.13

SCALE:

DO NOT SCALE DRAWING

SHEET 95 OF 167

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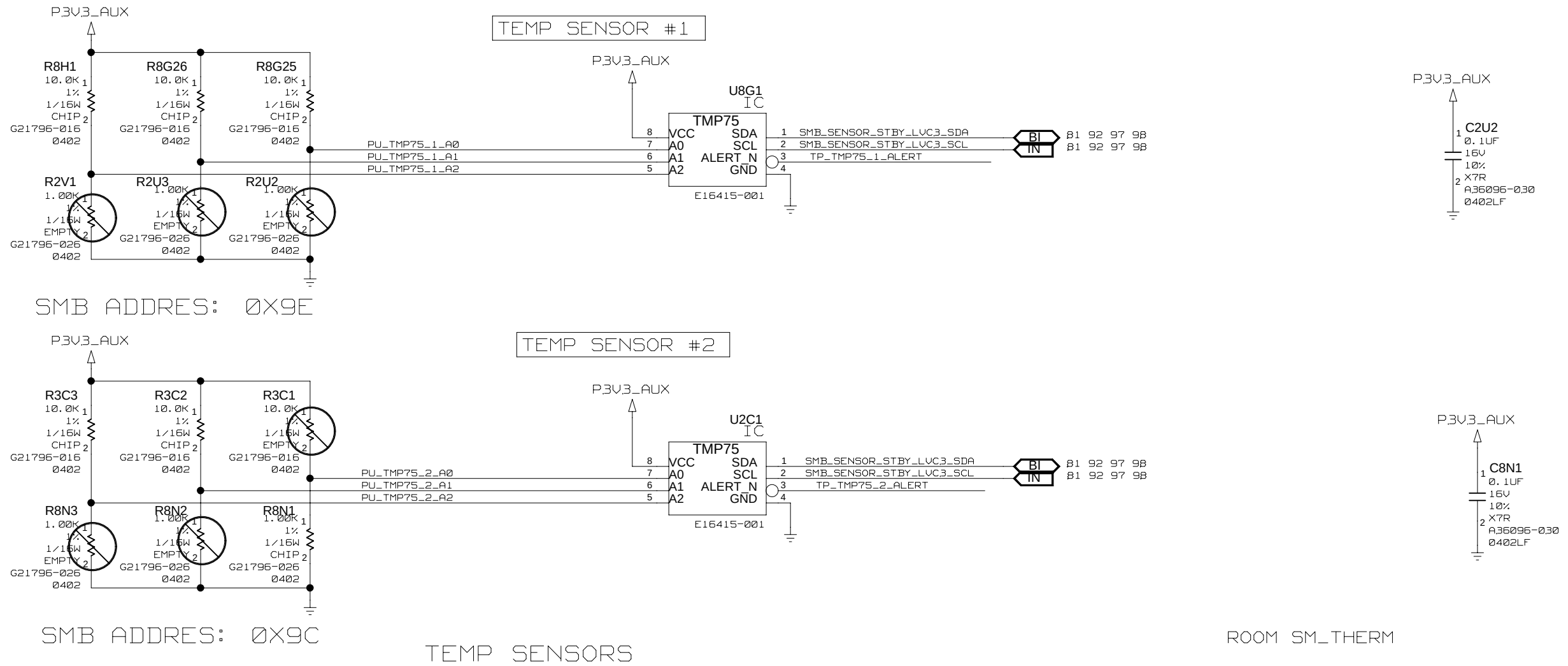


ROOM: BMC

BMC AVIN

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		SCALE:		DO NOT SCALE DRAWING		SHEET 96 OF 167



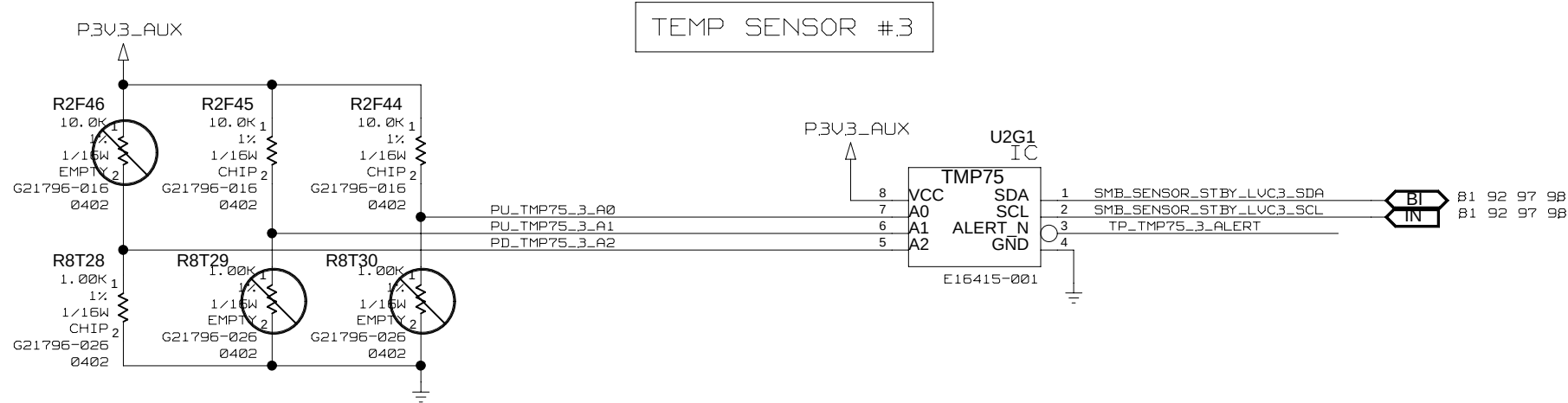
WHEN A SENSOR IS PLACED NEAR A COMPONENT, THE SENSOR MUST BE WITHIN .3MM

ROOM: TEMP_SENSE_X

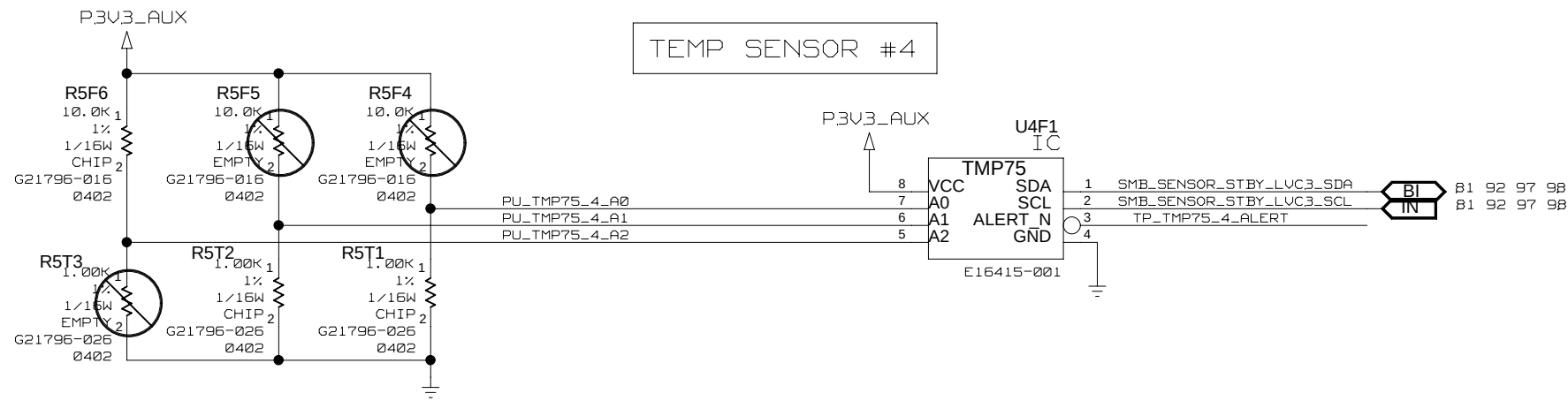
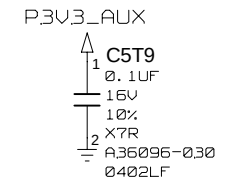
BMC TEMP SENSORS

Thu Nov 17 15:19:32 2016

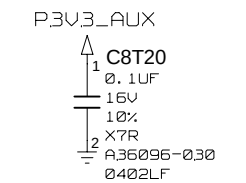
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
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SCALE:		DO NOT SCALE DRAWING			SHEET 97 OF 167



SMB ADDRES: 0X96



SMB ADDRES: 0X98



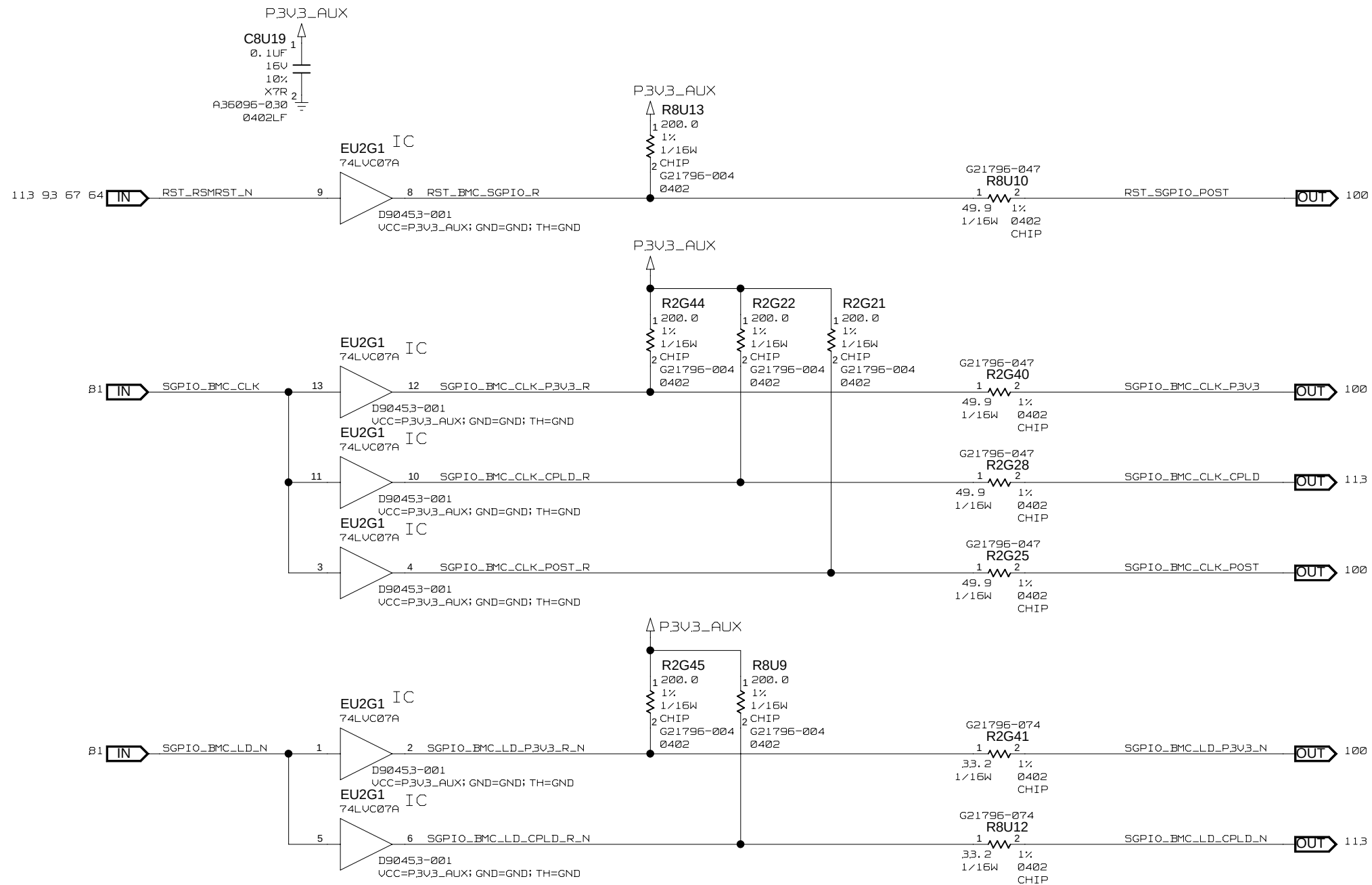
ROOM: TEMP_SENSE_X

BMC TEMP SENSORS

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ROOM: BMC_SGPIO
BOM_COST: SMLED

BMC_SGPIO (1 OF 2)

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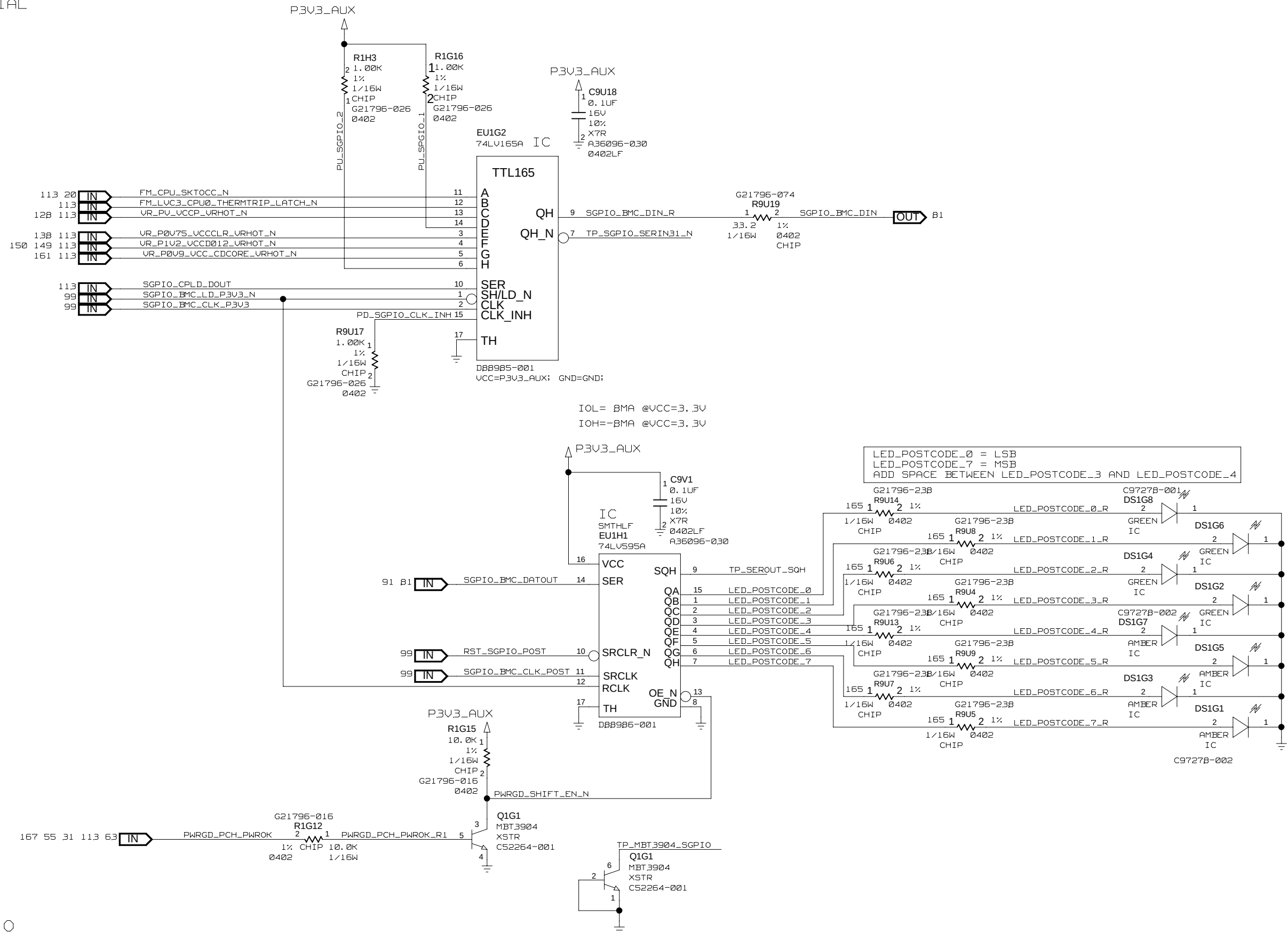
DOCUMENT NUMBER
G9428608

REV
.3.13

SCALE:

DO NOT SCALE DRAWING

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ROOM: BMC_SGPIO
BOM_COST: SM_LLED

BMC SGPIO (2 OF 2)

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CODE
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DOCUMENT NUMBER
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REV
3.13

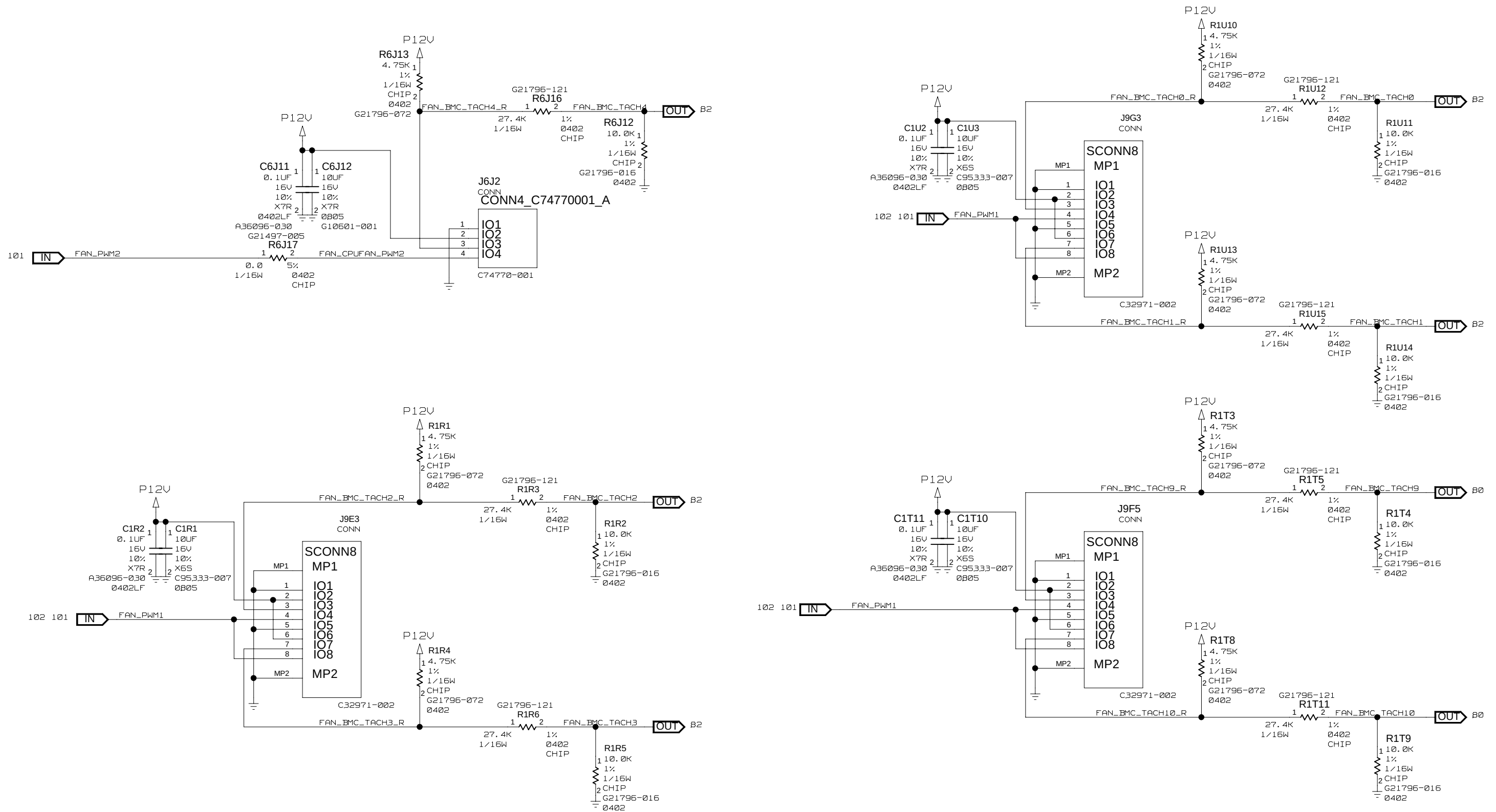
SCALE:

DO NOT SCALE DRAWING

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ROOM: FAN_CONNECTORS

SYS FAN CONNECTORS

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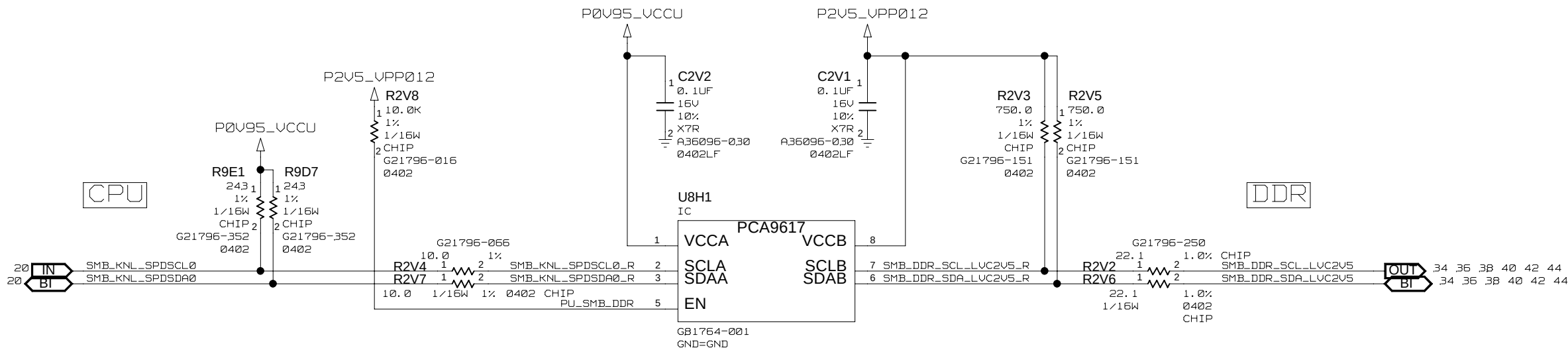
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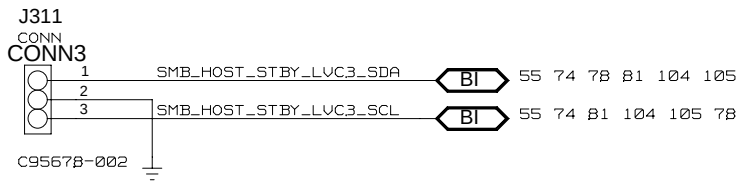
SHEET 102 OF 167

INTEL CONFIDENTIAL

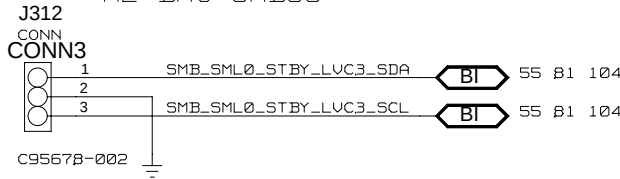
ROOM: MEM_SMBUS



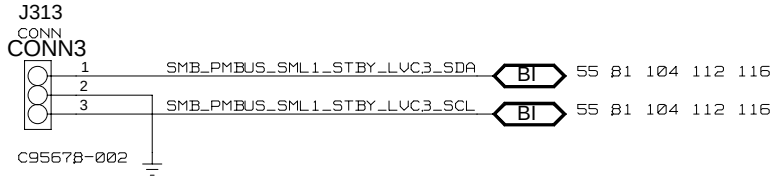
HOST SMBUS



ME-BMC SMBUS



POWER SUPPLY SMBUS



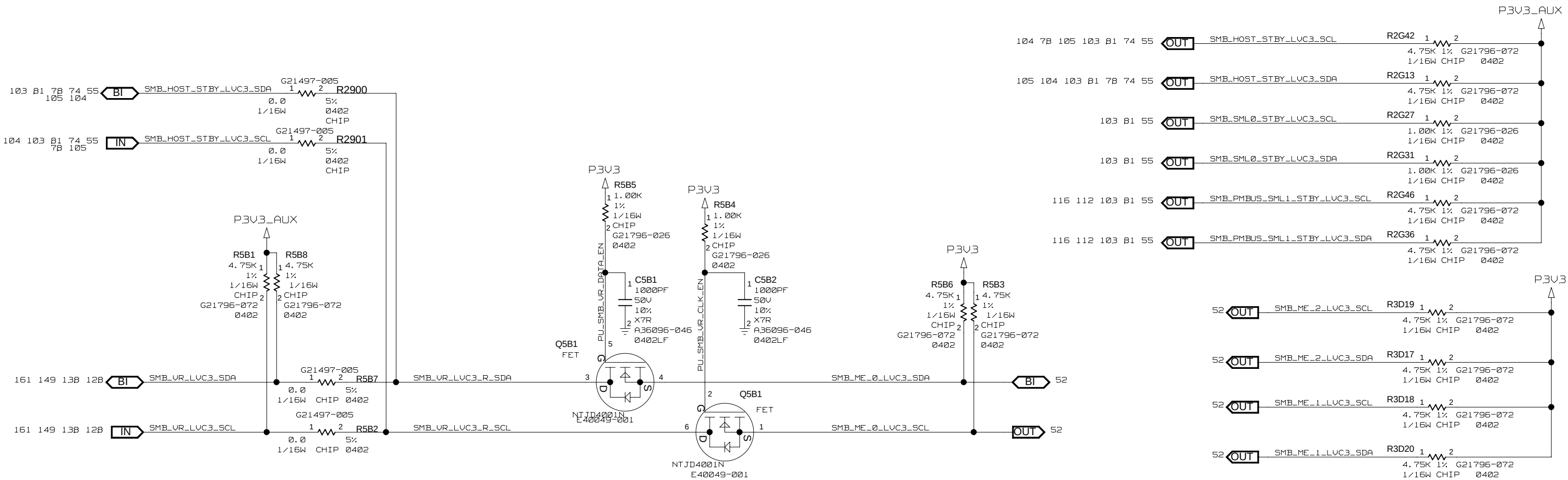
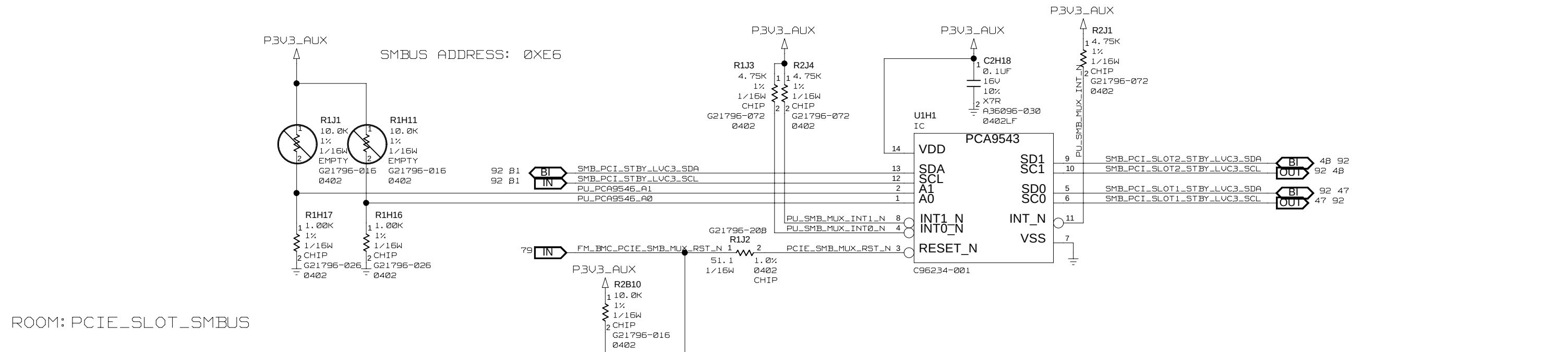
ROOM: SMBUS DEBUG

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SMBUS LEVEL-SHIFTER

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SCALE:		DO NOT SCALE DRAWING			SHEET 103 OF 167

SMBUS MUX FOR PCI SLOT

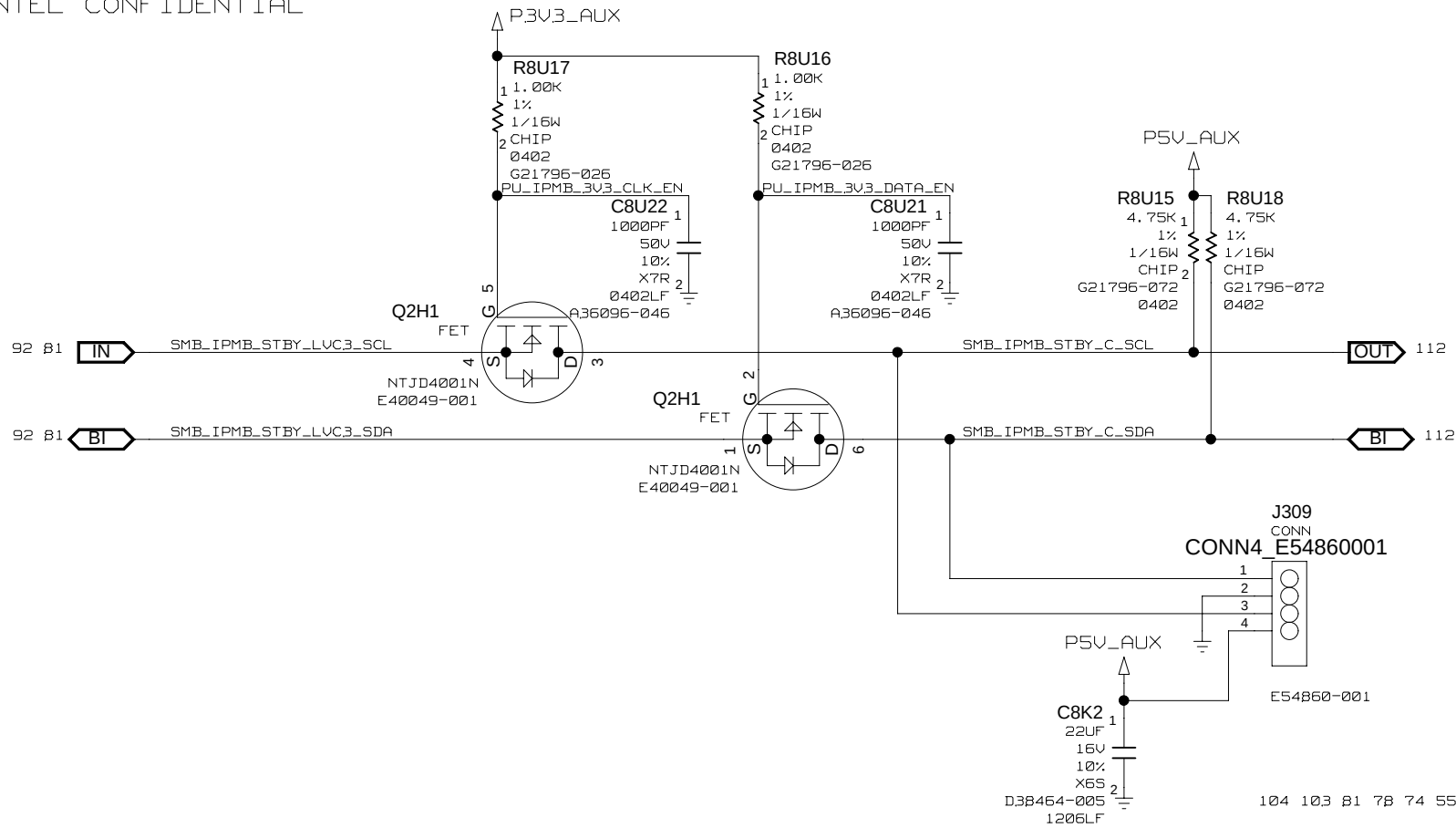


ROOM: PCH_SMBUS

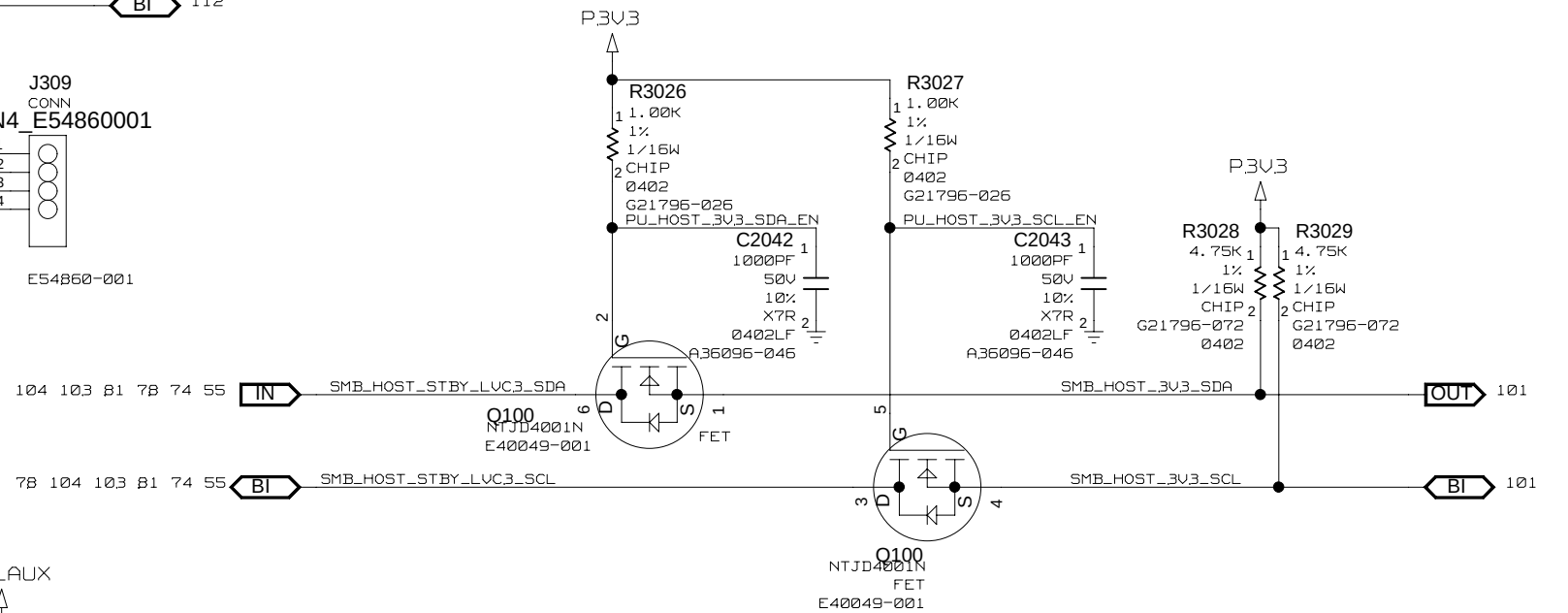
SMBUS MUX

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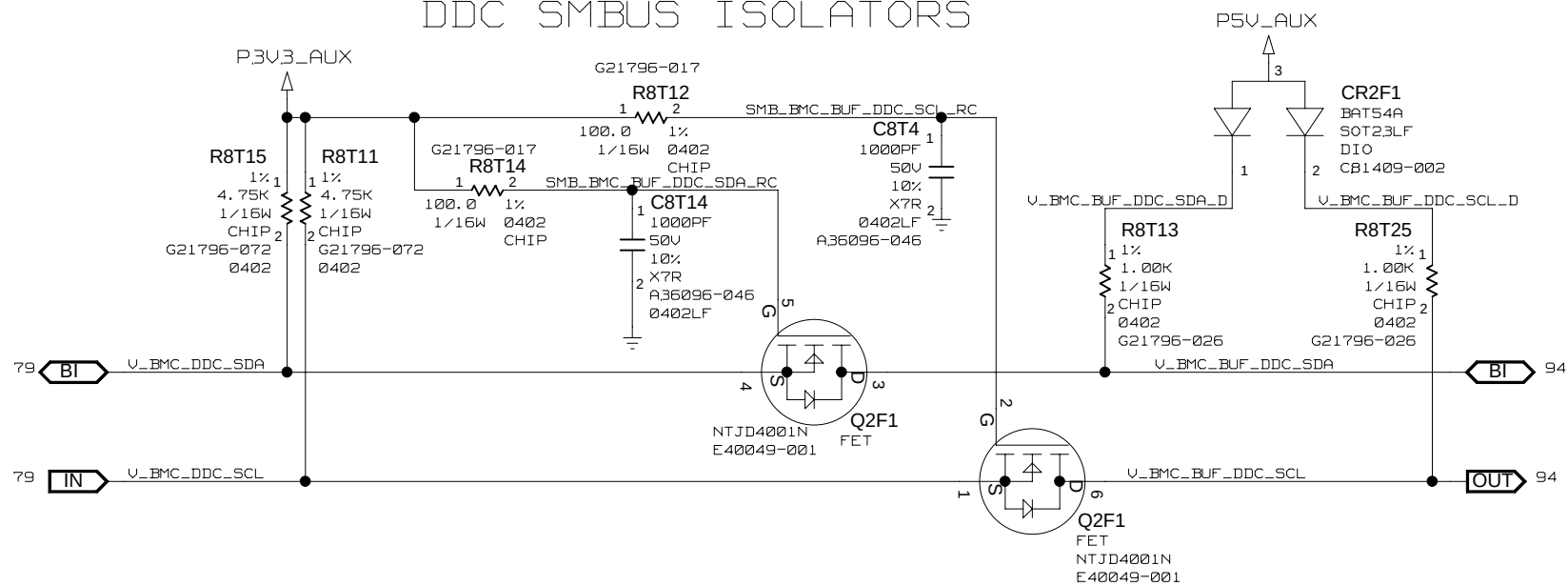
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
CBED	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	G9428608	3.13
SCALE:		DO NOT SCALE DRAWING			SHEET 104 OF 167



NPB SMBUS ISOLATORS



DDC SMBUS ISOLATORS



ROOM: BMC_SMBUS

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SMBUS ISOLATION

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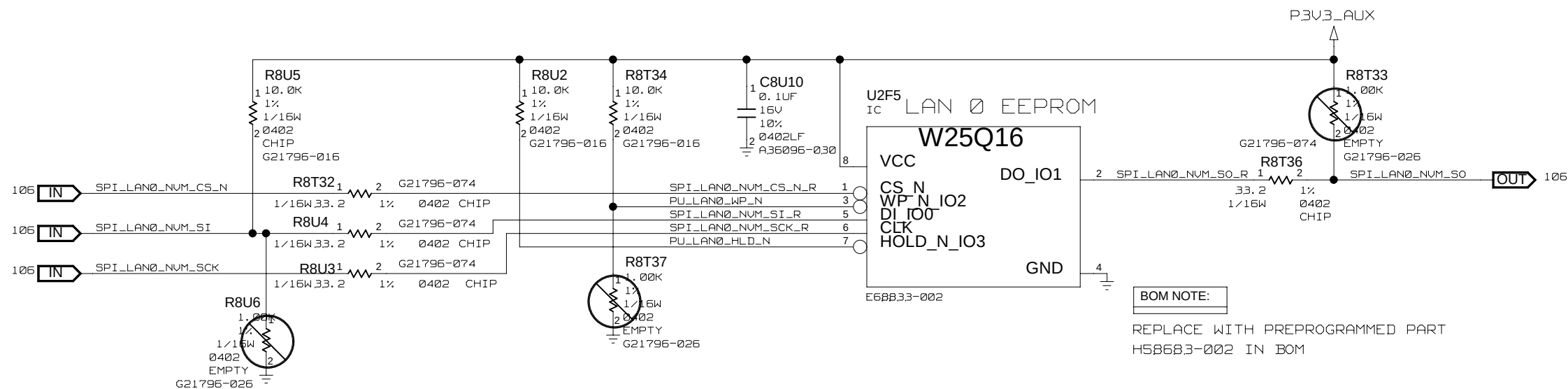
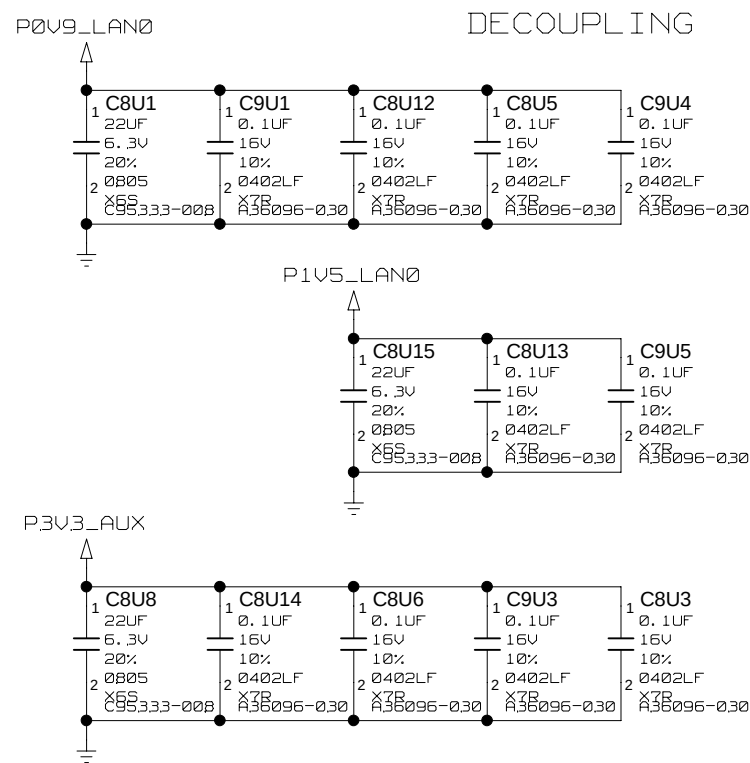
DOCUMENT NUMBER
G9428608

REV
.3.13

SCALE:

DO NOT SCALE DRAWING

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ROOM: LAN0

SPRINGVILLE 0 (2 OF 2)

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CODE

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DOCUMENT NUMBER

G9428608

REV

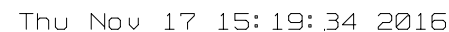
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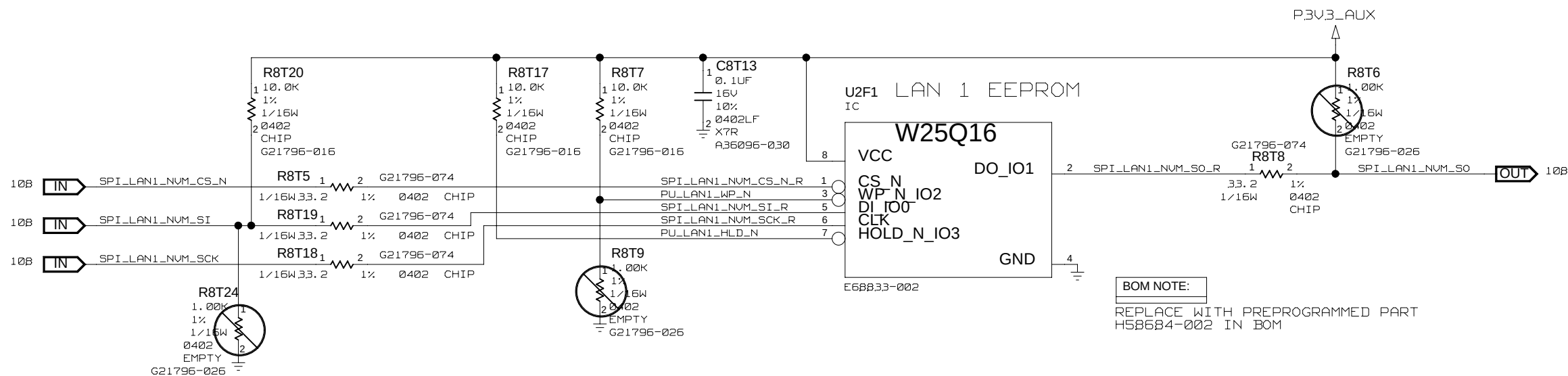
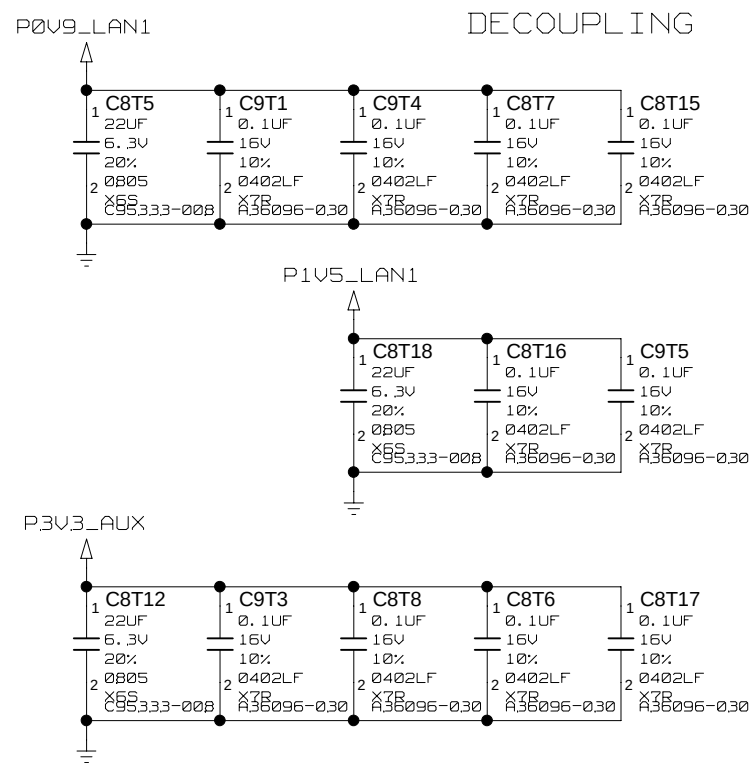
DO NOT SCALE DRAWING

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SPRINGVILLE



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ROOM: LAN1

SPRINGVILLE 1 (2 OF 2)

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CODE

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DOCUMENT NUMBER

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REV

.3.13

SCALE:

DO NOT SCALE DRAWING

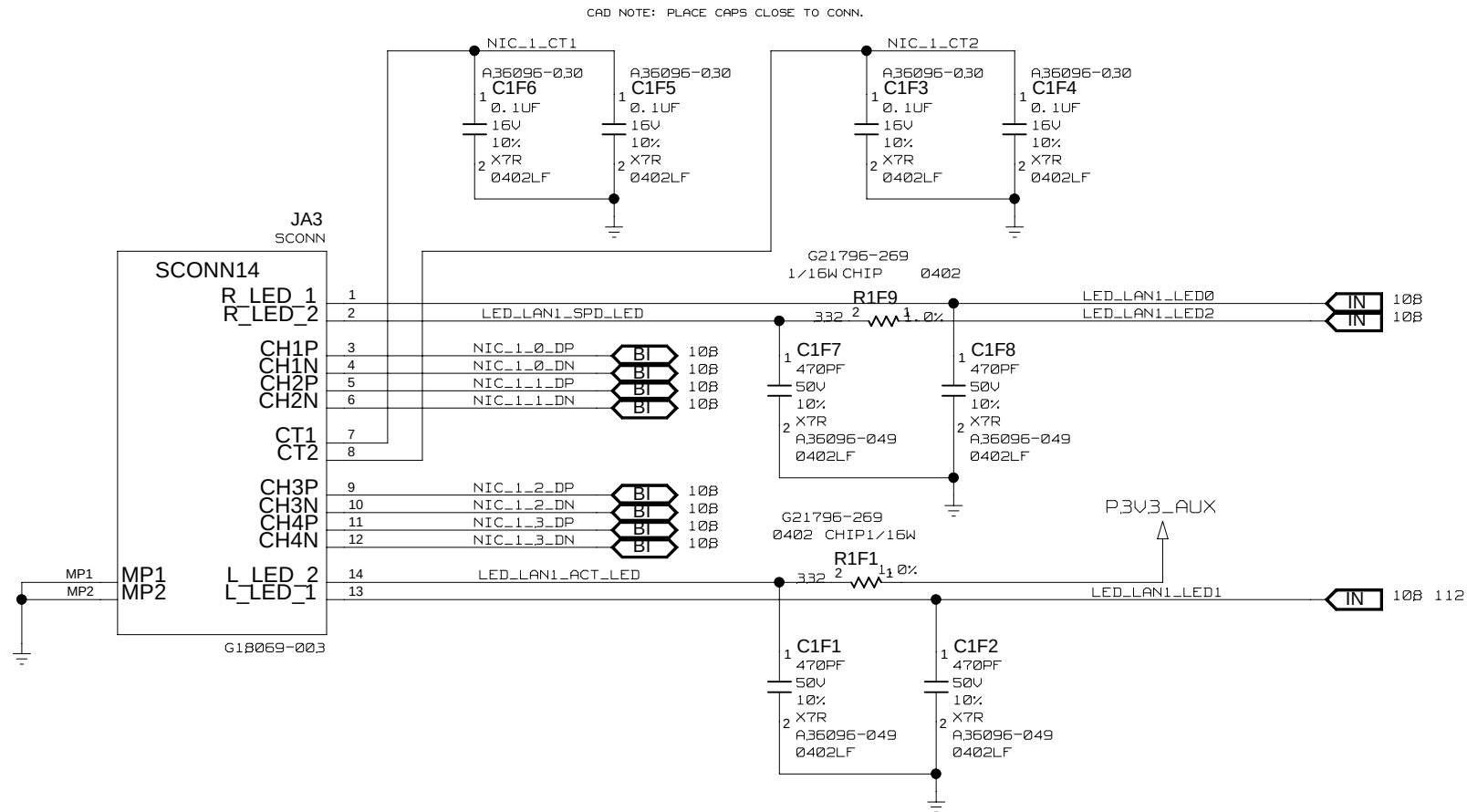
SHEET 109 OF 167

B

A

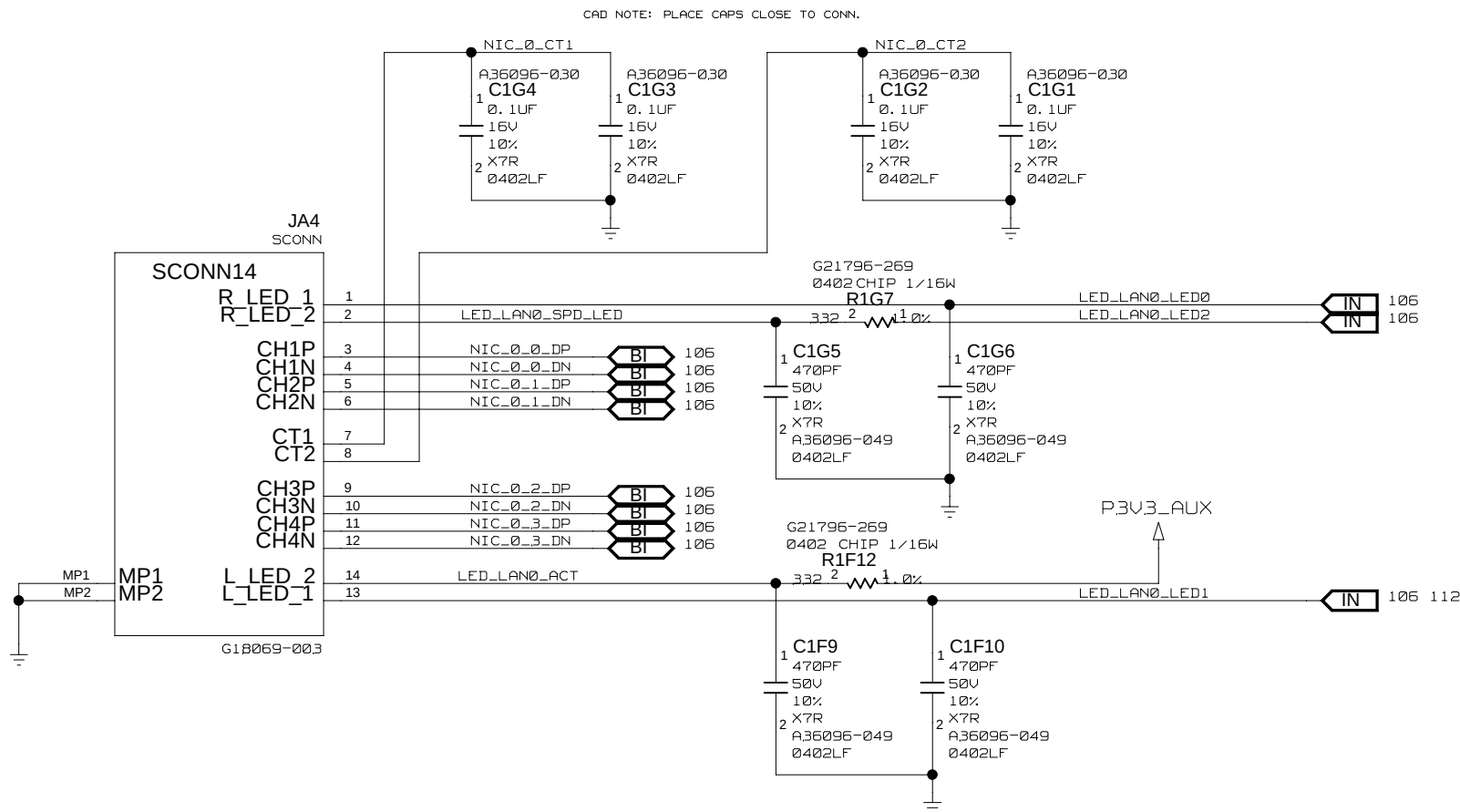
B

A



LEFT LED = LINK / ACTIVITY LED
OFF = NO LINK
GREEN = LINK, NO ACTIVITY
BLINKING GREEN = LINK, ACTIVITY

RIGHT LED = SPEED LED
OFF = 10 MBPS
ORANGE = 100 MBPS
GREEN = 1000 MBPS



ROOM: RJ45_CONNECTORS

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RJ45 CONNECTOR

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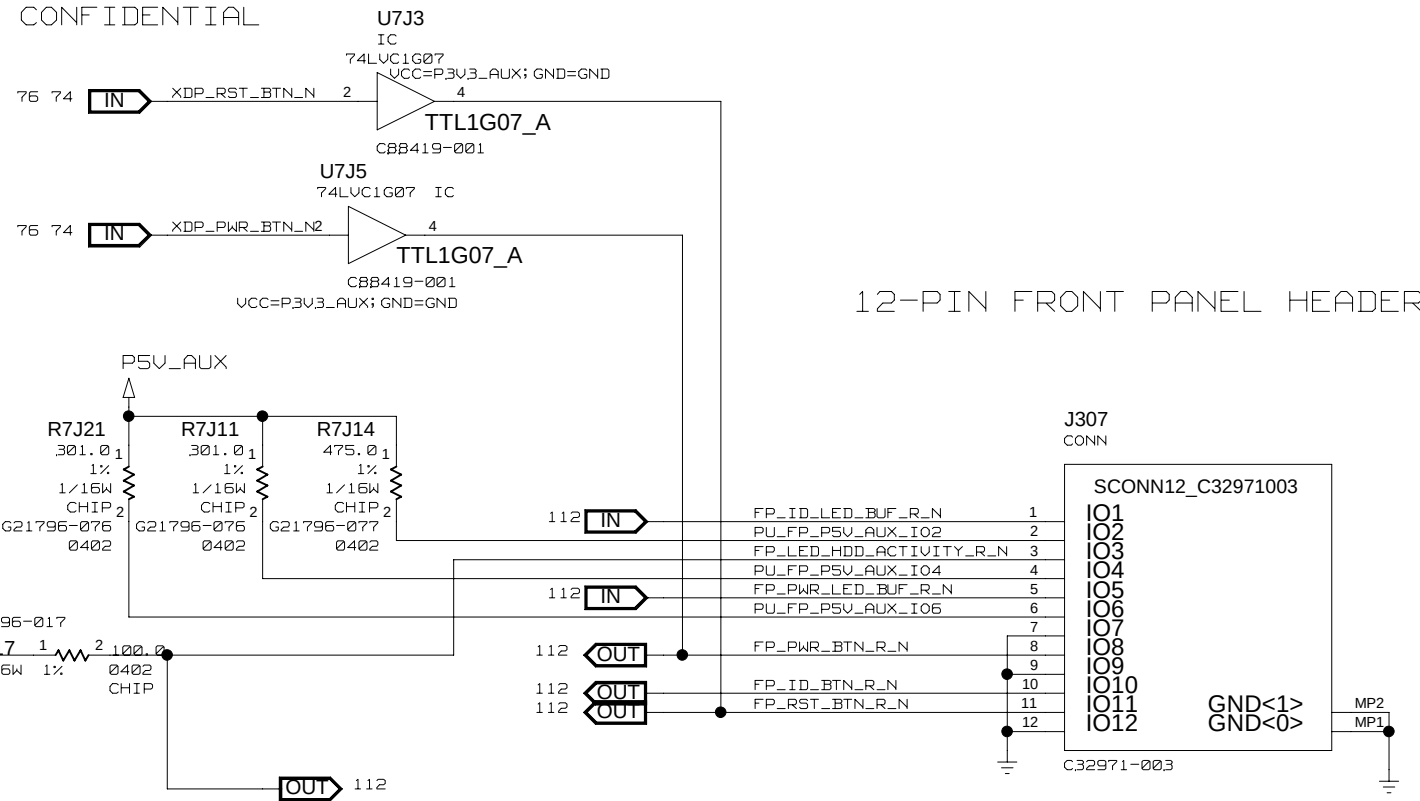
REV
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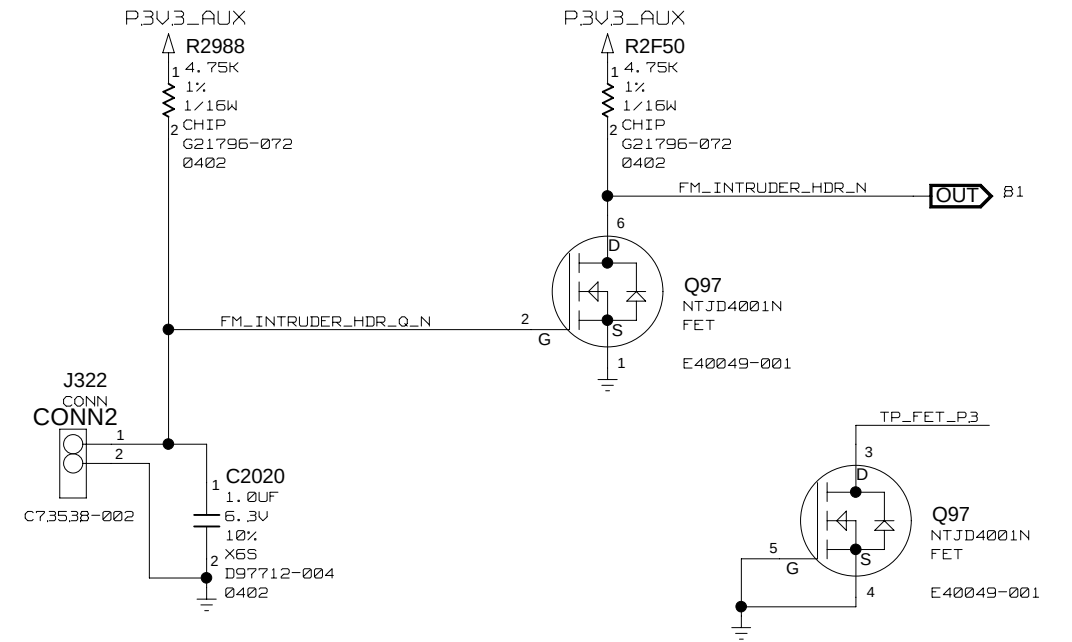
DO NOT SCALE DRAWING

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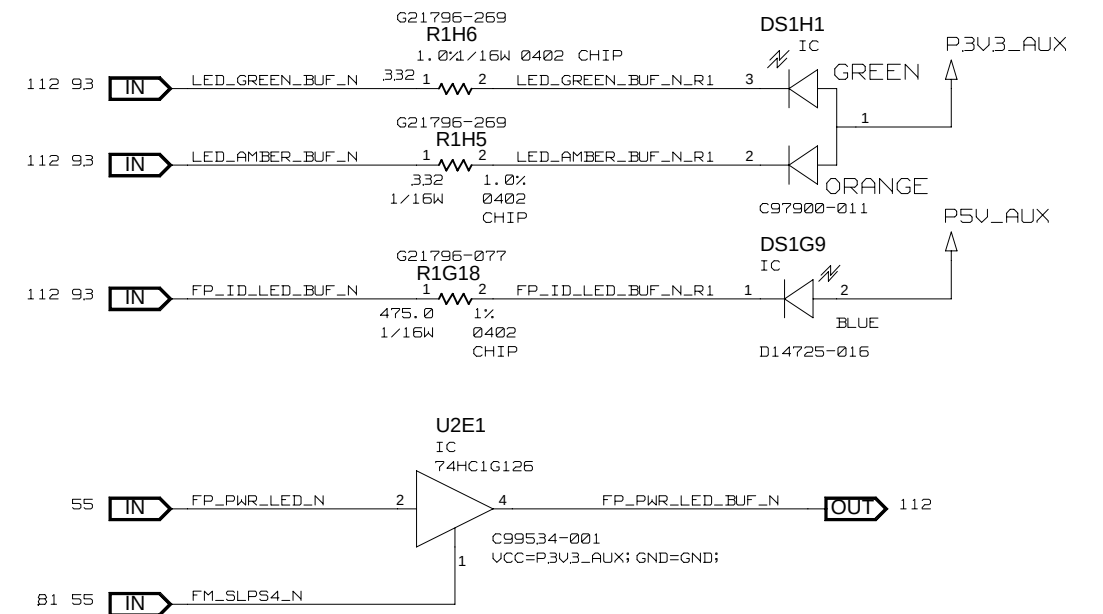
INTEL CONFIDENTIAL



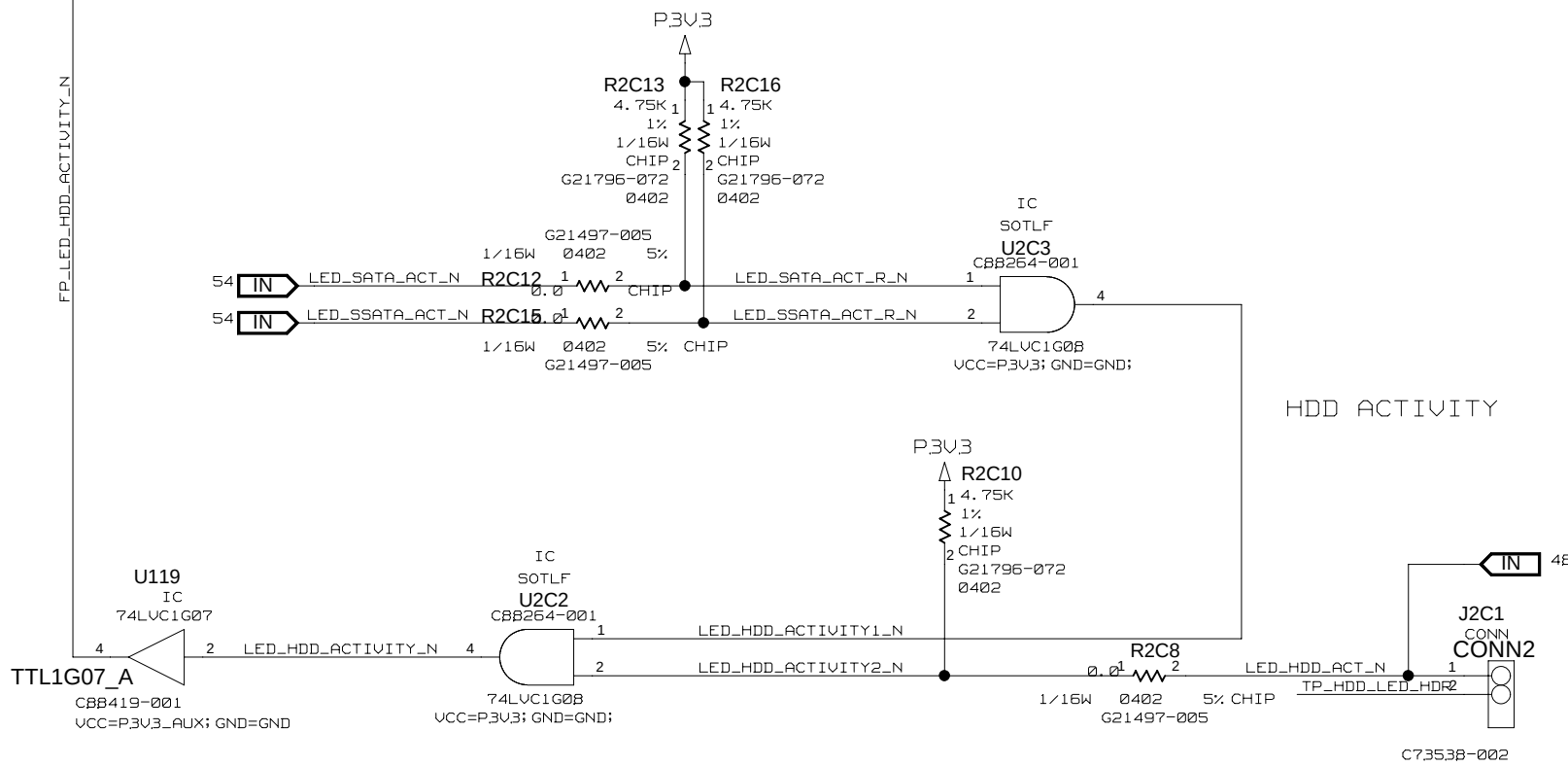
CHASSIS INTRUSION



STATUS AND ID LEDS



HDD ACTIVITY



ROOM: FP_CONN

FRONT PANEL HEADER/LEDS

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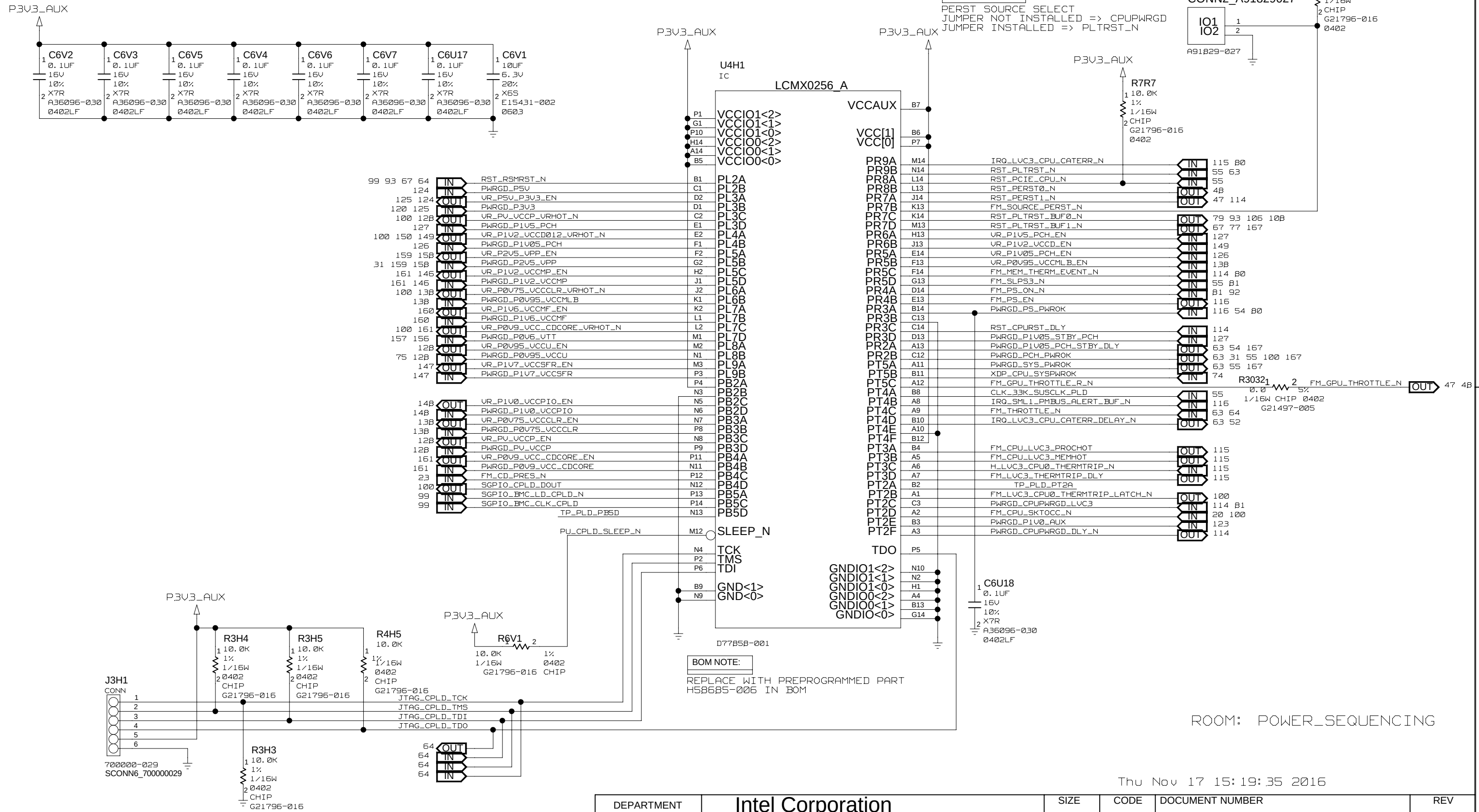
IO PINS C13 & N3 ARE CONNECTED TO GND TO IMPROVE CPLD BREAKOUT
IO PINS N13 & B2 ARE UNCONNECTED TO IMPROVE CPLD BREAKOUT
IO PINS P4 & B12 ARE CONNECTED TO VCCPIO TO SUPPORT LCMX0640
IO PINS N3 & A10 ARE CONNECTED TO GND TO SUPPORT LCMX0640

BOM NOTE:

ADD JUMPER A19527-001 TO BOM TO STUFF J1J5-1-2.

DESIGN NOTE:

PERST SOURCE SELECT
JUMPER NOT INSTALLED => CPUPWRGD
JUMPER INSTALLED => PLTRST_N



ROOM: POWER_SEQUENCING

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POWER SEQUENCING CPLD

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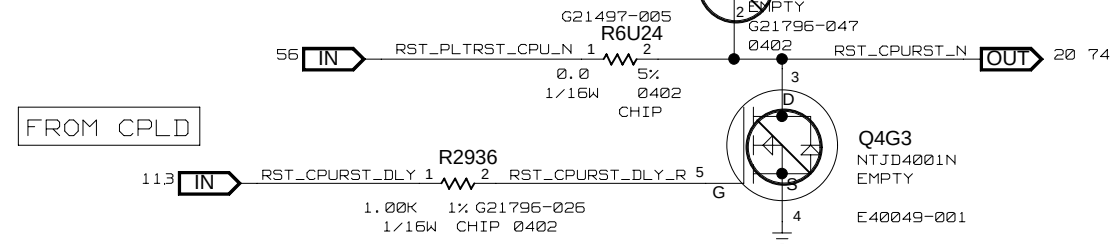
3.13

SCALE:

DO NOT SCALE DRAWING

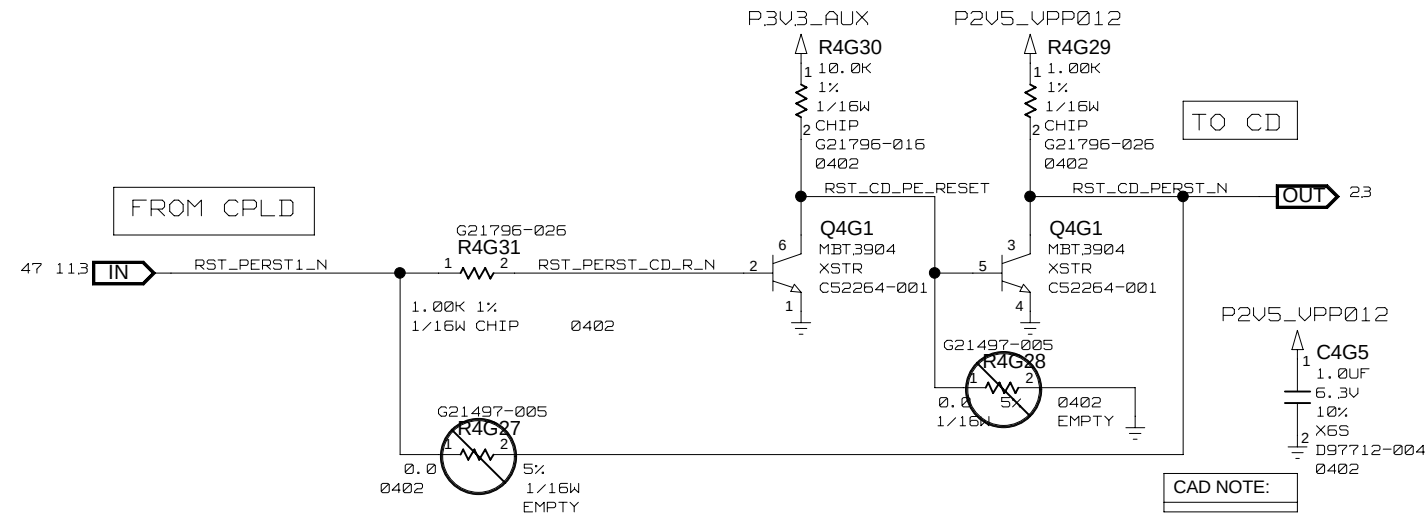
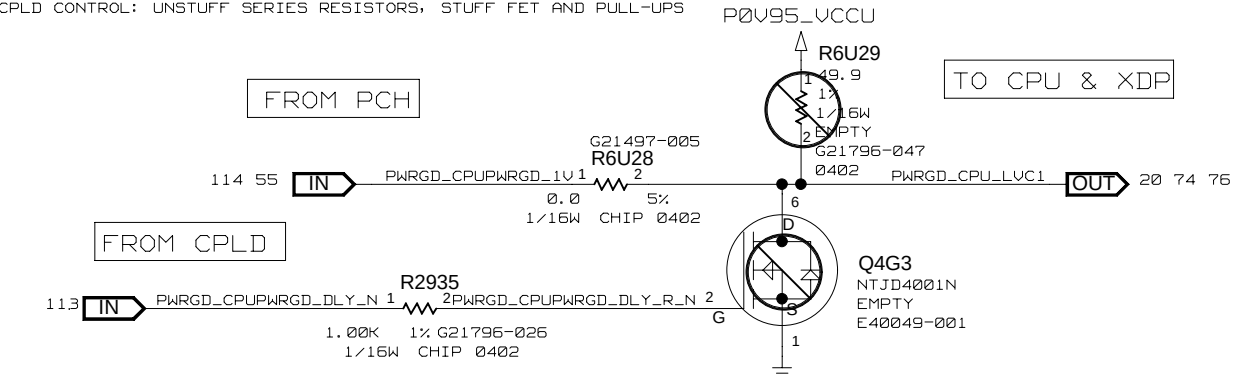
SHEET 113 OF 167

INTEL CONFIDENTIAL
ROOM: SIDEBAND-LT

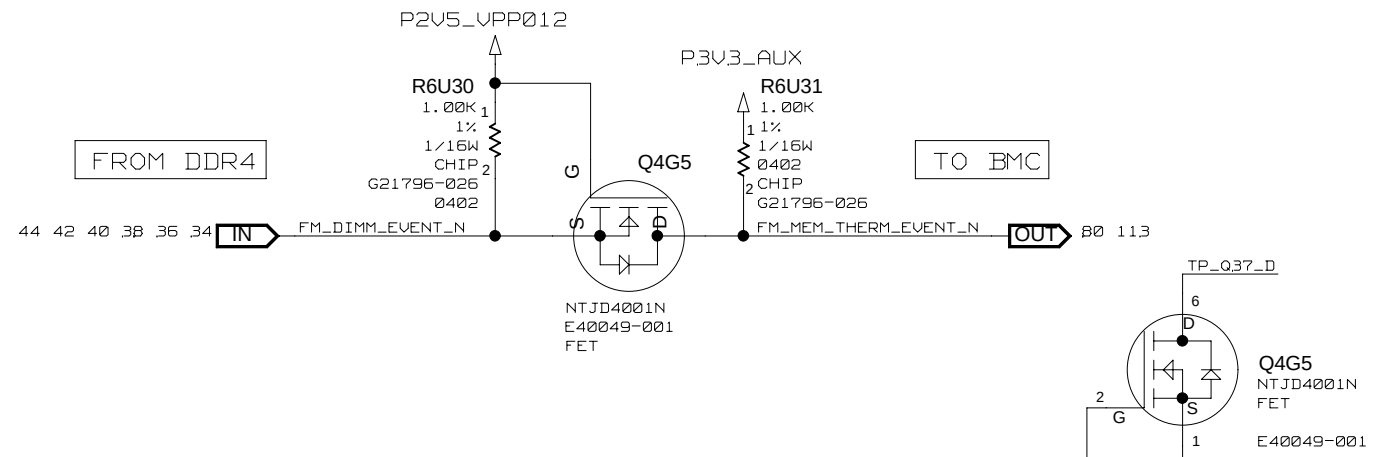
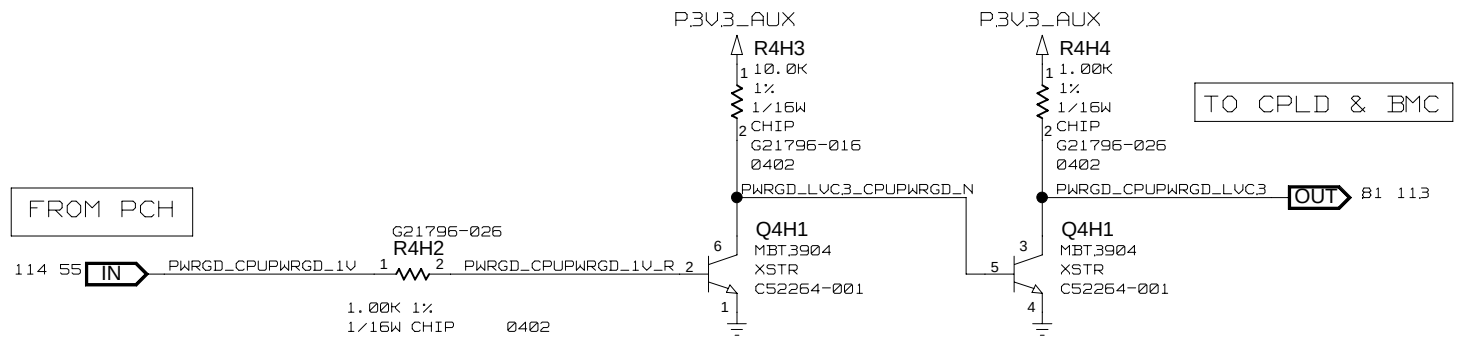
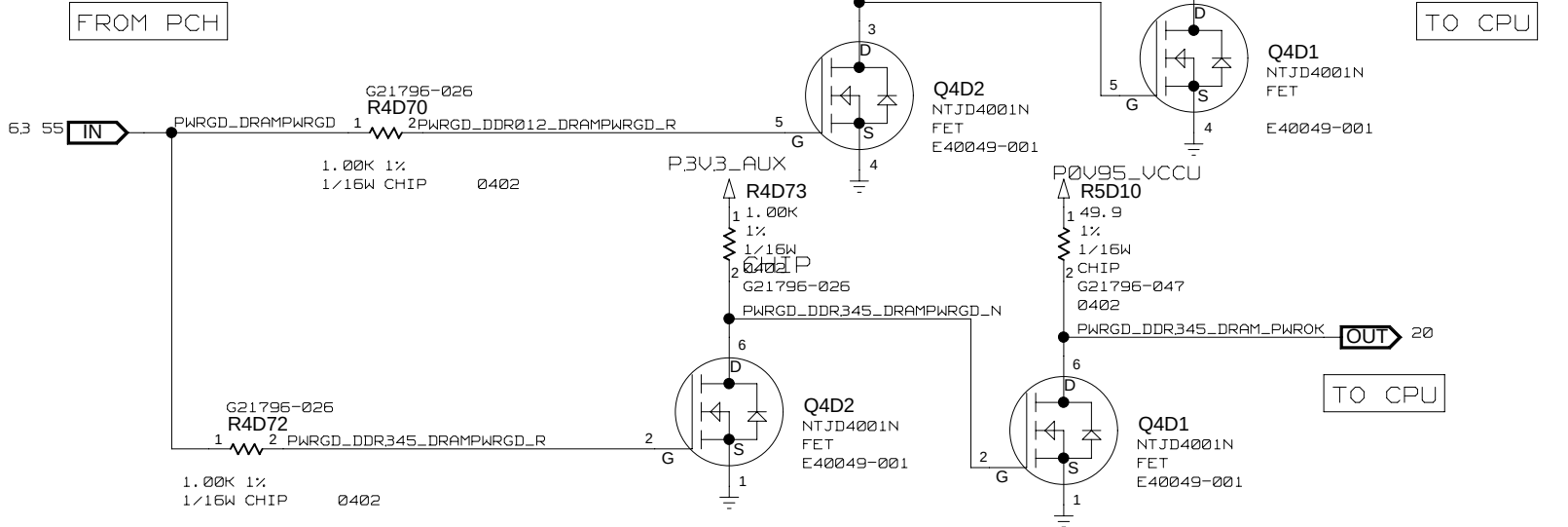


DESIGN NOTE:

CPU PLTRST AND PWRGD OVERRIDE
PCH CONTROL (DEFAULT): STUFF SERIES RESISTORS, UNSTUFF FET AND PULL-UPS
CPLD CONTROL: UNSTUFF SERIES RESISTORS, STUFF FET AND PULL-UPS



CAD NOTE:
PLACE NEAR Q4G1



SIDEBAND LEVEL-TRANSLATORS 1/2

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3.13

SCALE:

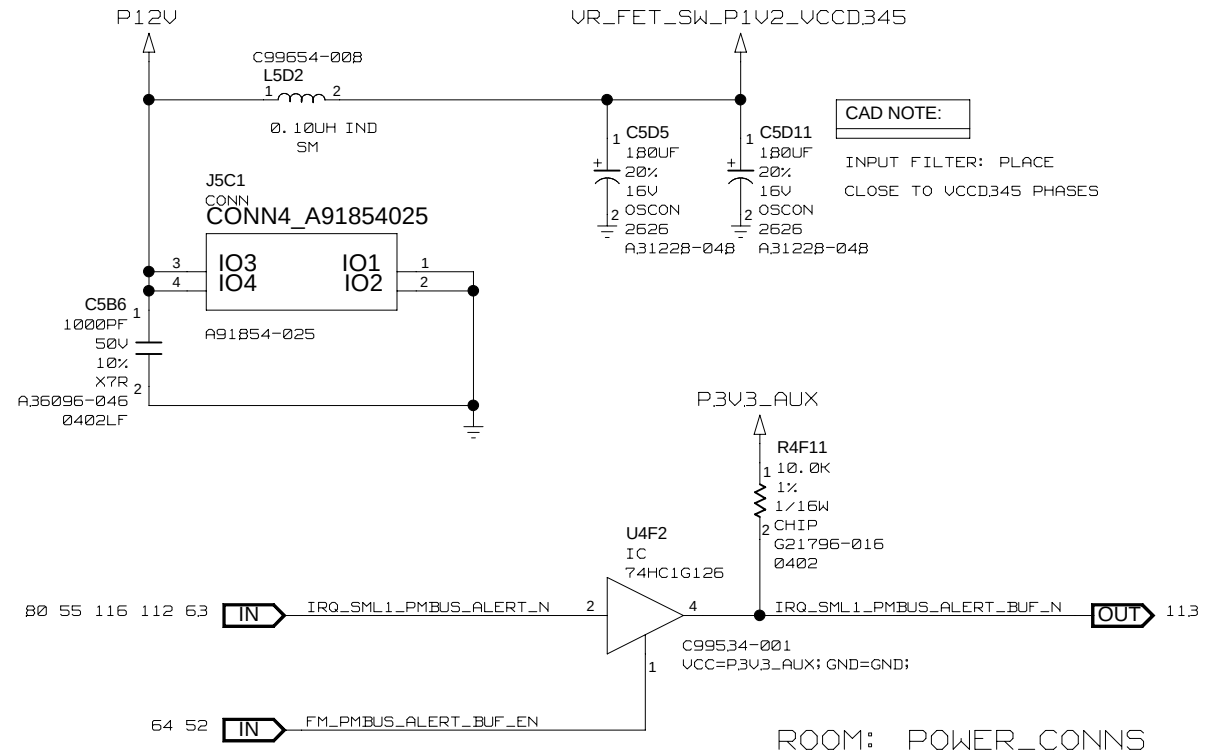
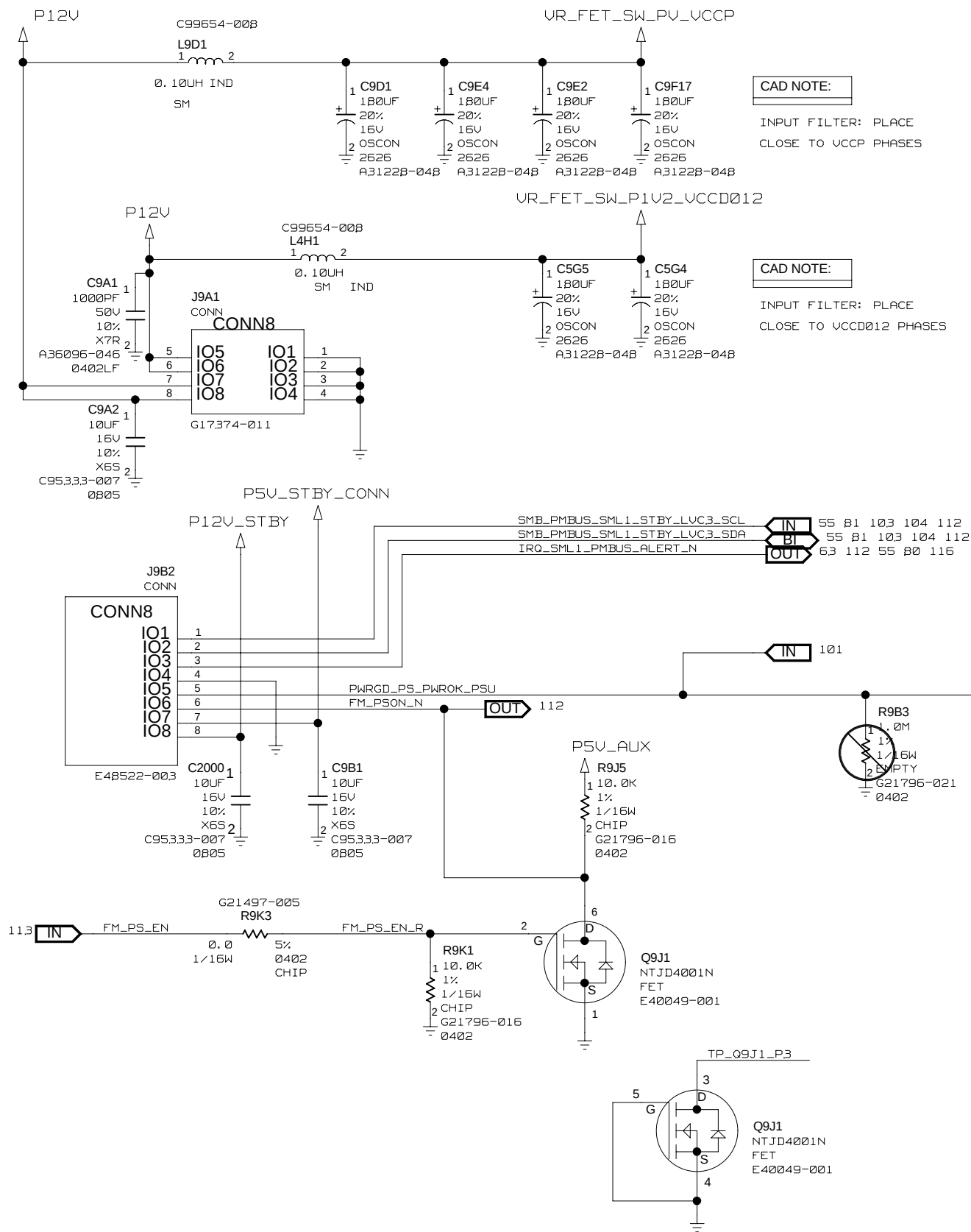
DO NOT SCALE DRAWING

SHEET 114 OF 167

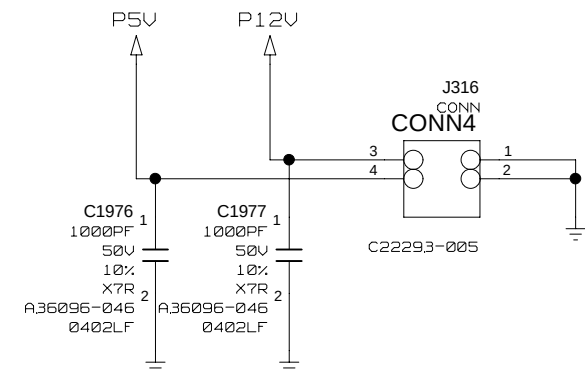


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DISK DRIVE POWER CONNECTOR



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POWER CONNECTORS

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3.13

SCALE:

DO NOT SCALE DRAWING

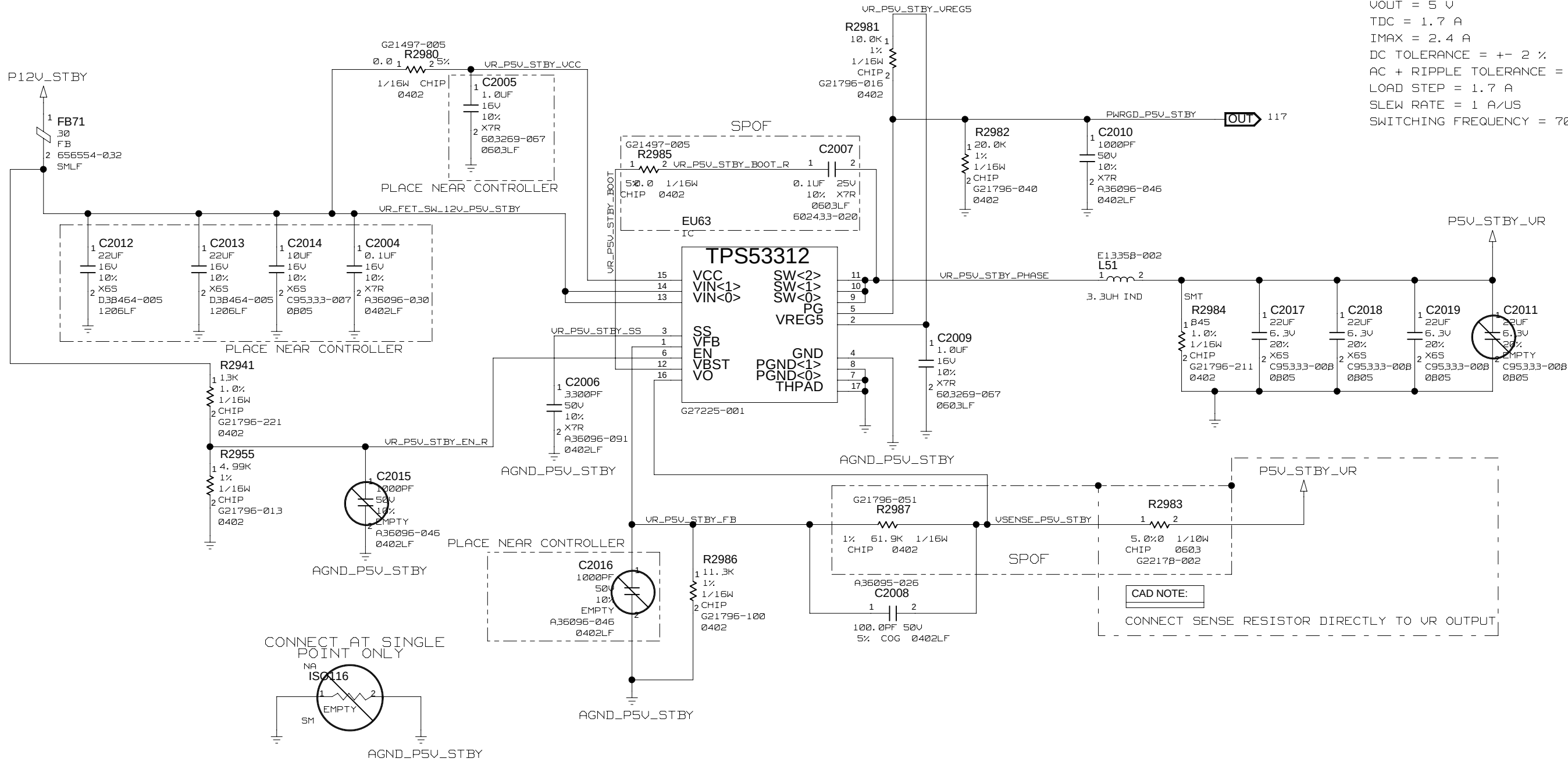
SHEET 116 OF 167



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DESIGN NOTE:

P5V_STBY VR SPECIFICATION
VOUT = 5 V
TDC = 1.7 A
IMAX = 2.4 A
DC TOLERANCE = $\pm 2\%$
AC + RIPPLE TOLERANCE = $\pm 3\%$
LOAD STEP = 1.7 A
SLEW RATE = 1 A/ μ S
SWITCHING FREQUENCY = 700 KHZ

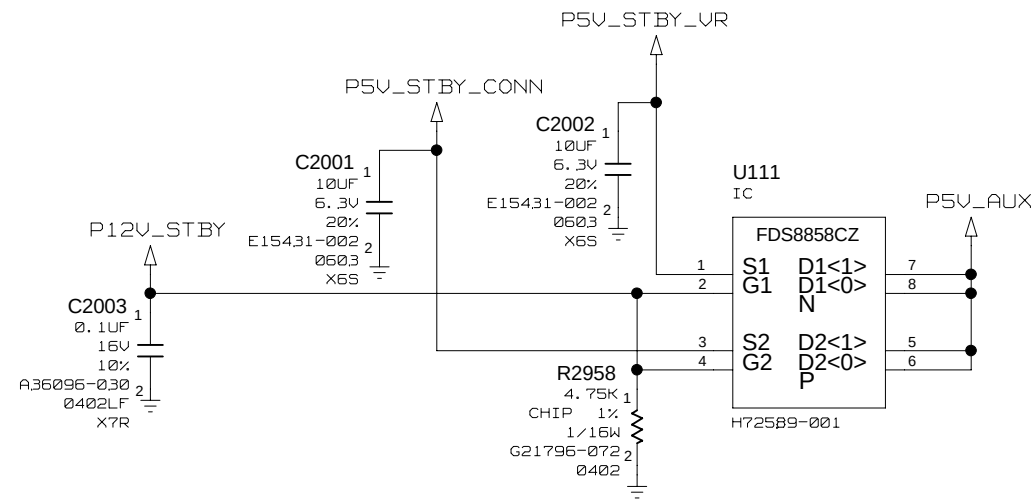


ROOM = P5V_STBY_VR
P5V_STBY VR

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SCALE:		DO NOT SCALE DRAWING			SHEET 118 OF 167

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P12V_STBY	P5V_AUX
0V 12V	P5V_STBY_CONN P5V_STBY_VR

ROOM: P5V_STBY_SW

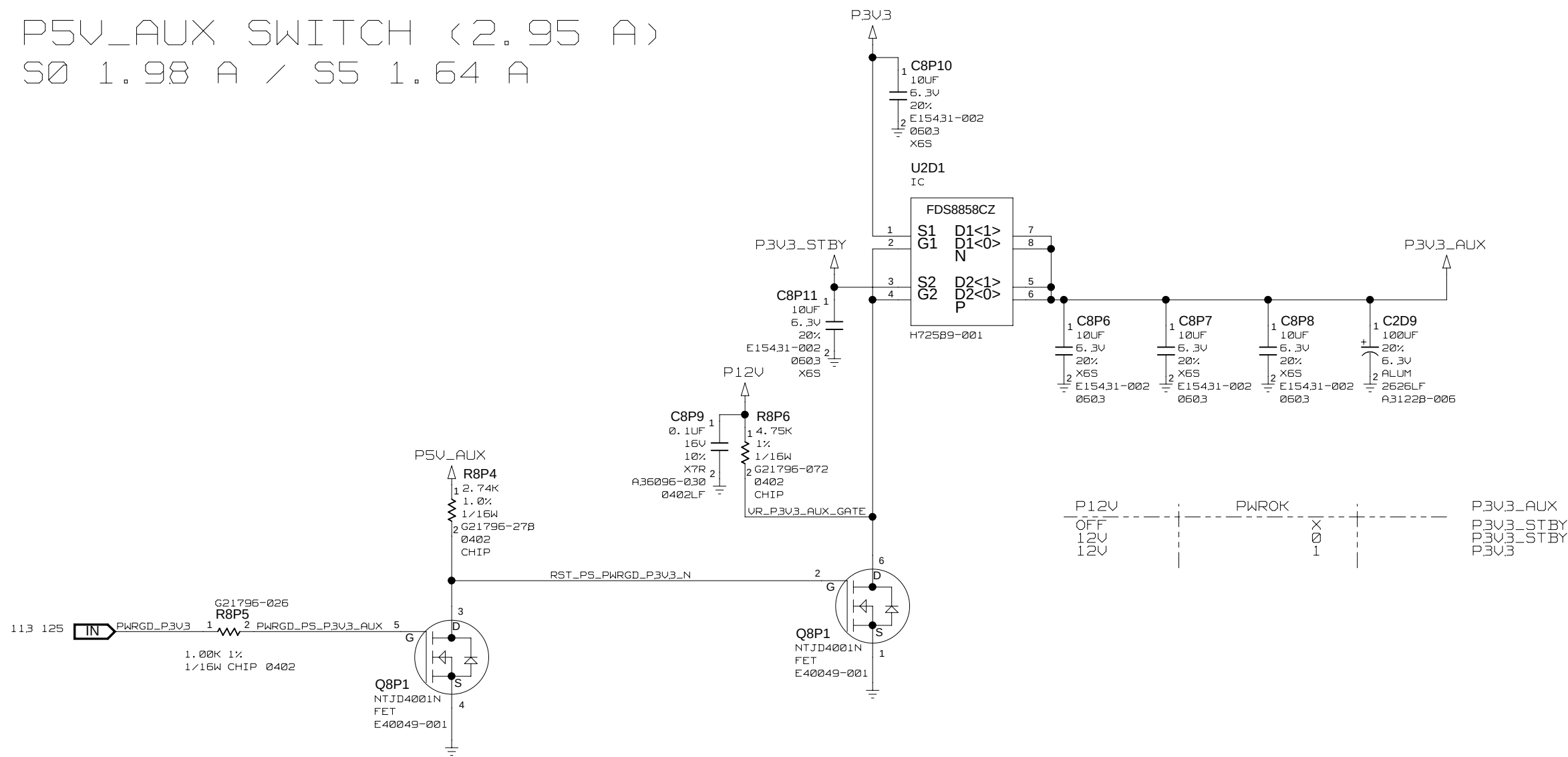
P5V_STBY SWITCH

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SCALE:		DO NOT SCALE DRAWING			SHEET 119 OF 167

P3V3_AUX SWITCH (3.74 A)
S0 2.56 A / S5 2.08 A

P5V_AUX SWITCH (2.95 A)
S0 1.98 A / S5 1.64 A

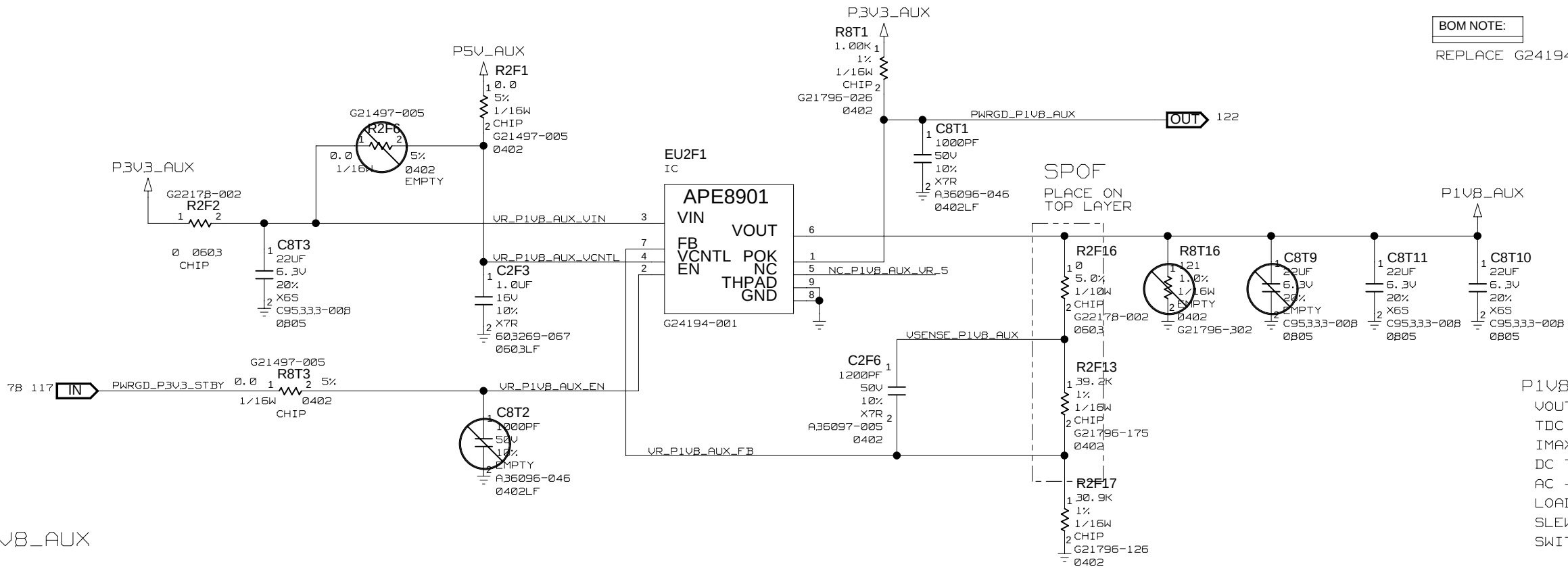


ROOM: P3V3_AUX_SW

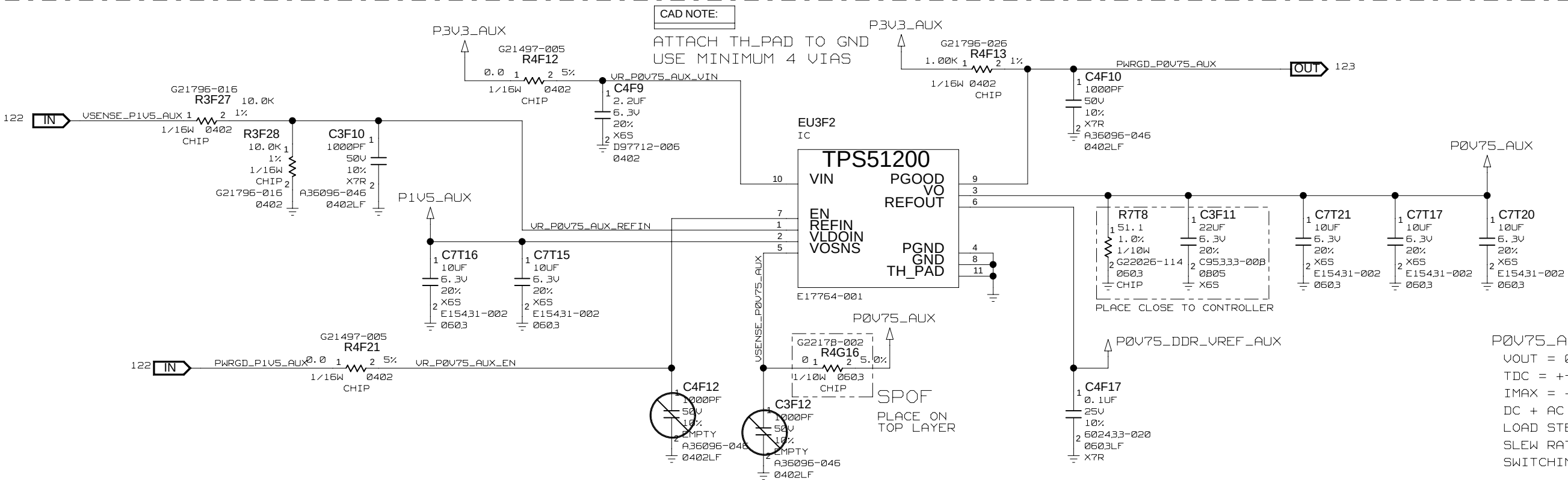
P3V3_AUX SWITCH

Thu Nov 17 15:19:36 2016

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
CBED	2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119	B	34649	G9428608	.3.13
SCALE:		DO NOT SCALE DRAWING			SHEET 120 OF 167



ROOM: VR_P1V8_AUX



ROOM: VR_P0V75_AUX

P1V8_AUX & P0V75_AUX VRS

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2200 MISSION COLLEGE BLVD.
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SIZE
B

CODE
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DOCUMENT NUMBER
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REV
3.13

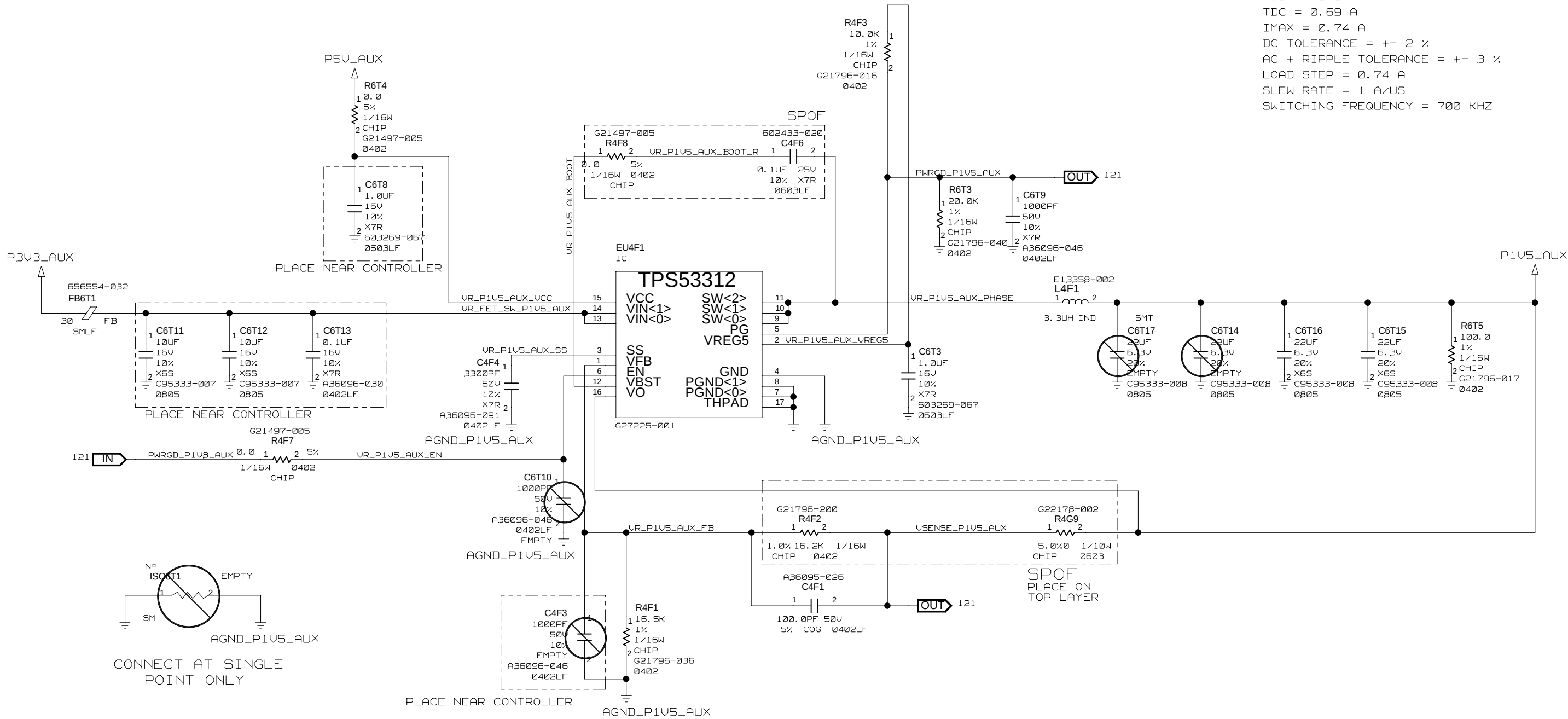
SCALE:

DO NOT SCALE DRAWING

SHEET 121 OF 167

DESIGN NOTE:

P1V5_AUX VR SPECIFICATION
VOUT = 1.5 V
TDC = 0.69 A
IMAX = 0.74 A
DC TOLERANCE = +- 2 %
AC + RIPPLE TOLERANCE = +- 3 %
LOAD STEP = 0.74 A
SLEW RATE = 1 A/US
SWITCHING FREQUENCY = 700 KHZ



ROOM: VR_P1V5_AUX

P1V5_AUX VR

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SCALE:		DO NOT SCALE DRAWING			SHEET 122 OF 167

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DESIGN NOTE:

P1V0_AUX VR SPECIFICATION

$$V_{OUT} = 1.0 \text{ V}$$
$$TDC = 0.72 \text{ A}$$
$$I_{MAX} = 0.84 \text{ A}$$

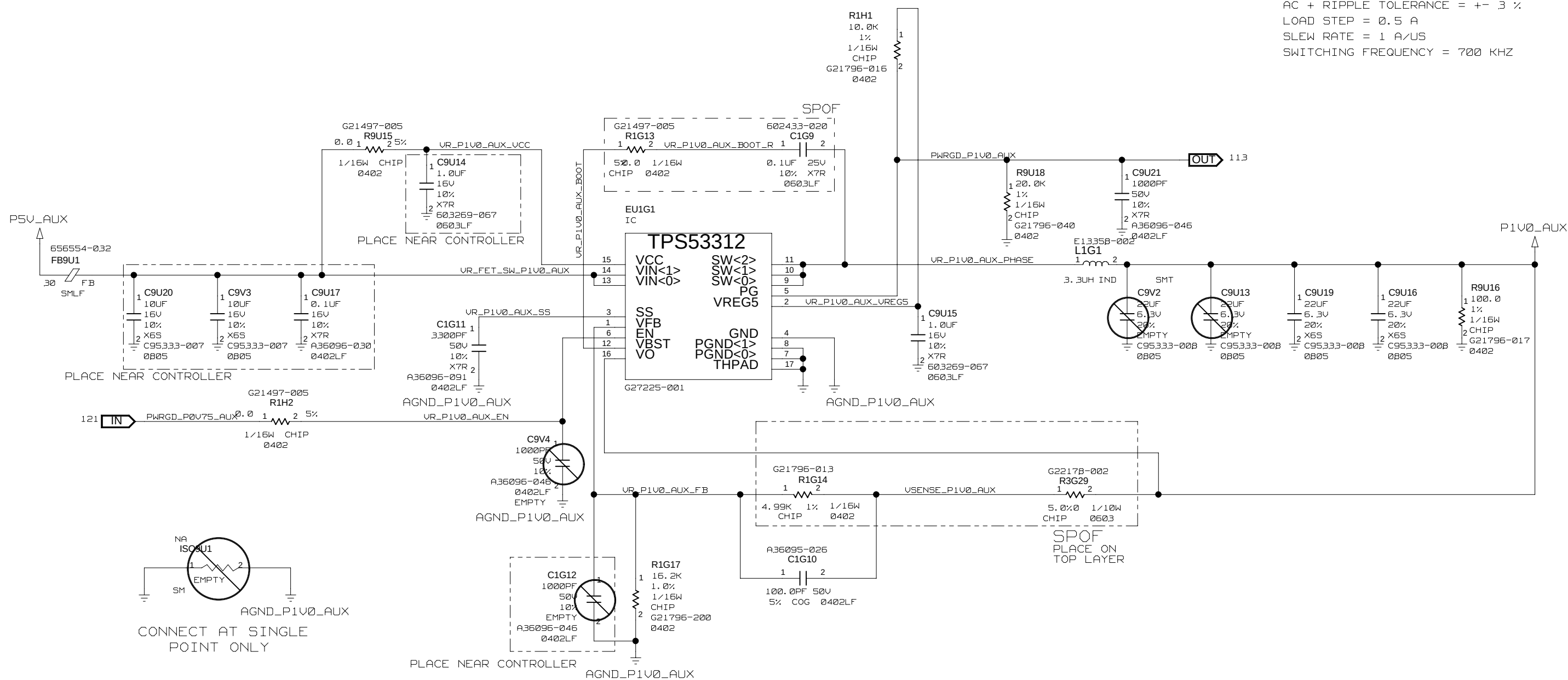
DC TOLERANCE = $\pm 2\%$

$$AC + RIPPLE \text{ TOLERANCE} = \pm .3 \%$$

LOAD STEP = 0.5 A

SLEW RATE = 1 A/US

SWITCHING FREQUENCY = 700 KHZ



ROOM: VR_P1V0_AUX

P1V0_AUX VR

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2200 MISSION COLLEGE BLVD.
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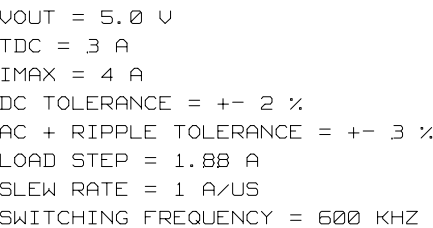
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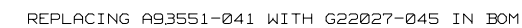
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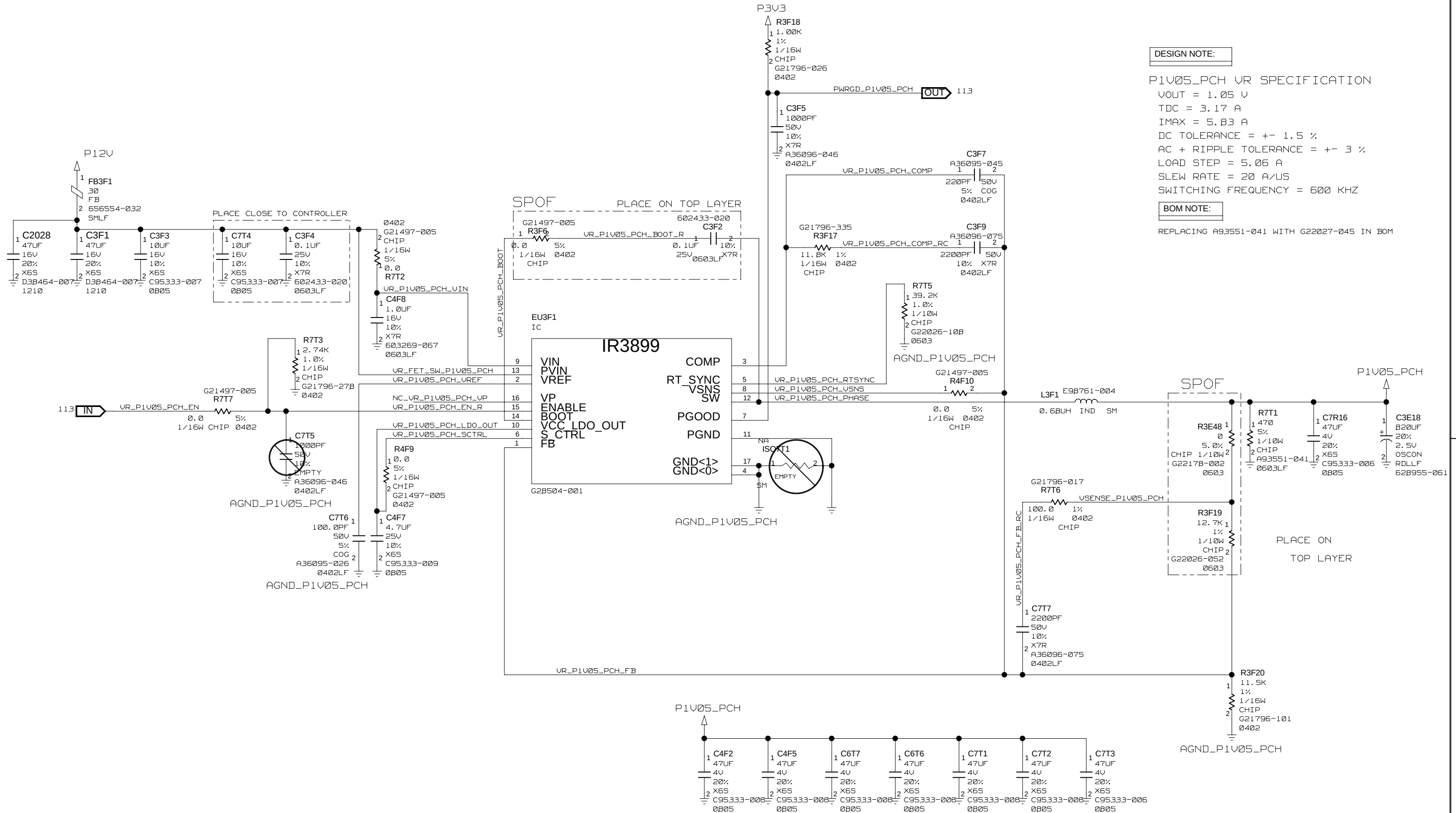
SCALE:

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ROOM: VR_P1V05_PCH

P1V05_PCH VR

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		SCALE:		DO NOT SCALE DRAWING	SHEET 126 OF 167	

CAD NOTE:

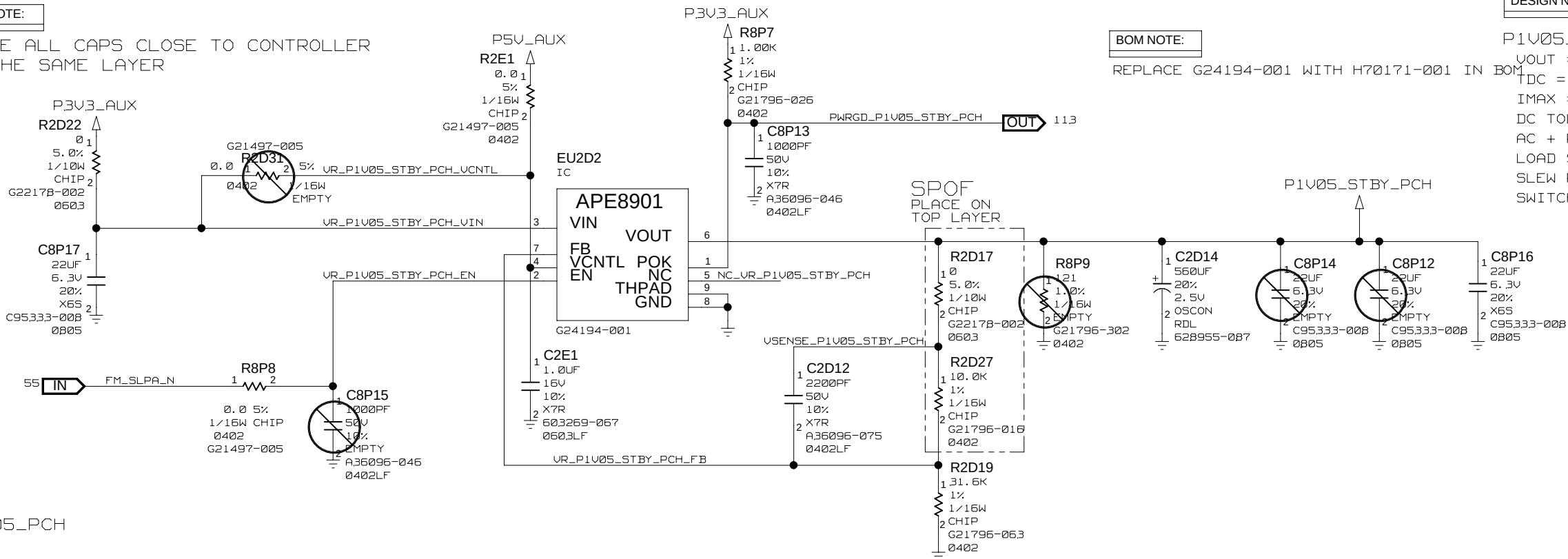
PLACE ALL CAPS CLOSE TO CONTROLLER
ON THE SAME LAYER

DESIGN NOTE:

P1V05_STBY_PCH VR SPECIFICATION
VOUT = 1.05 V
TDC = 0.11 A
IMAX = 0.67 A
DC TOLERANCE = +- 1.5 %
AC + RIPPLE TOLERANCE = +- .3 %
LOAD STEP = 0.67 A
SLEW RATE = 1 A/US
SWITCHING FREQUENCY = NA (LINEAR)

BOM NOTE:

REPLACE G24194-001 WITH H70171-001 IN BOM



ROOM: VR_P1V05_PCH

CAD NOTE:

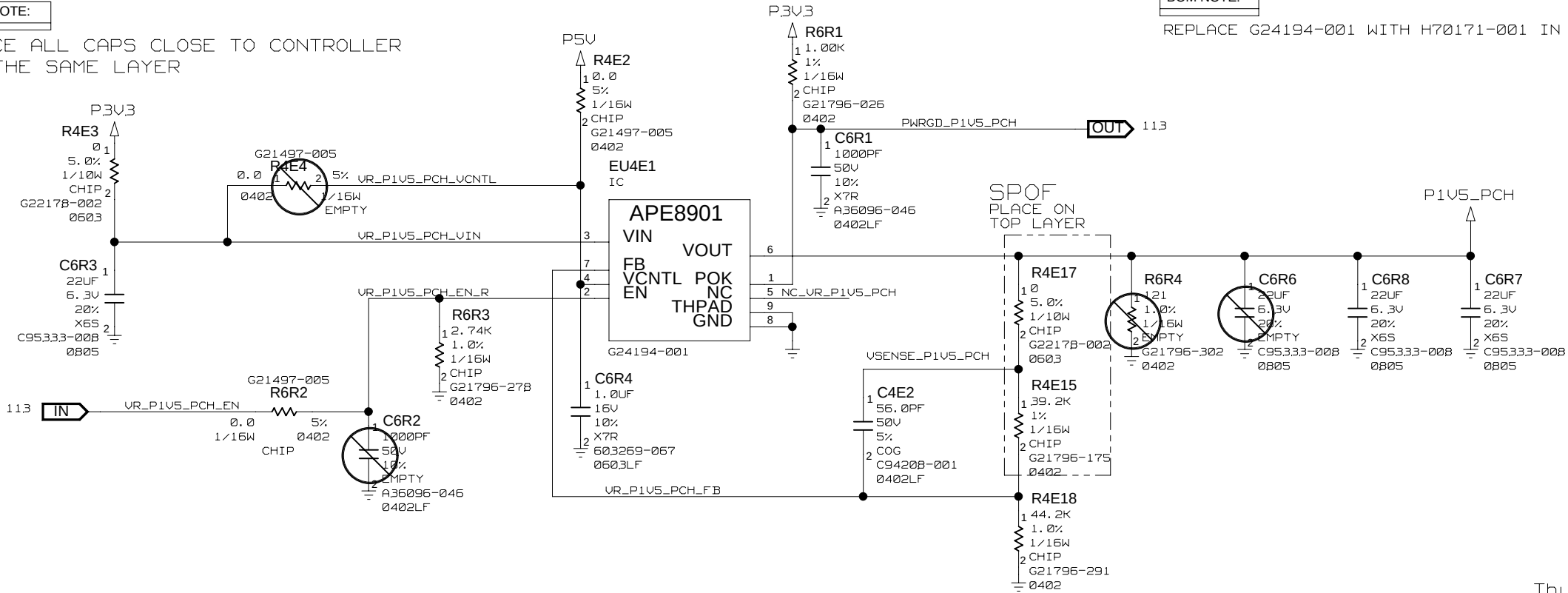
PLACE ALL CAPS CLOSE TO CONTROLLER
ON THE SAME LAYER

DESIGN NOTE:

P1V5_PCH VR SPECIFICATION
VOUT = 1.5 V
TDC = 0.15 A
IMAX = 0.19 A
DC TOLERANCE = +- 1.5 %
AC + RIPPLE TOLERANCE = +- .3 %
LOAD STEP = 0.03 A
SLEW RATE = 1 A/US
SWITCHING FREQUENCY = NA (LINEAR)

BOM NOTE:

REPLACE G24194-001 WITH H70171-001 IN BOM



ROOM: VR_P1V05_PCH

P1V05_STBY_PCH & P1V5_PCH VRS

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SCALE:

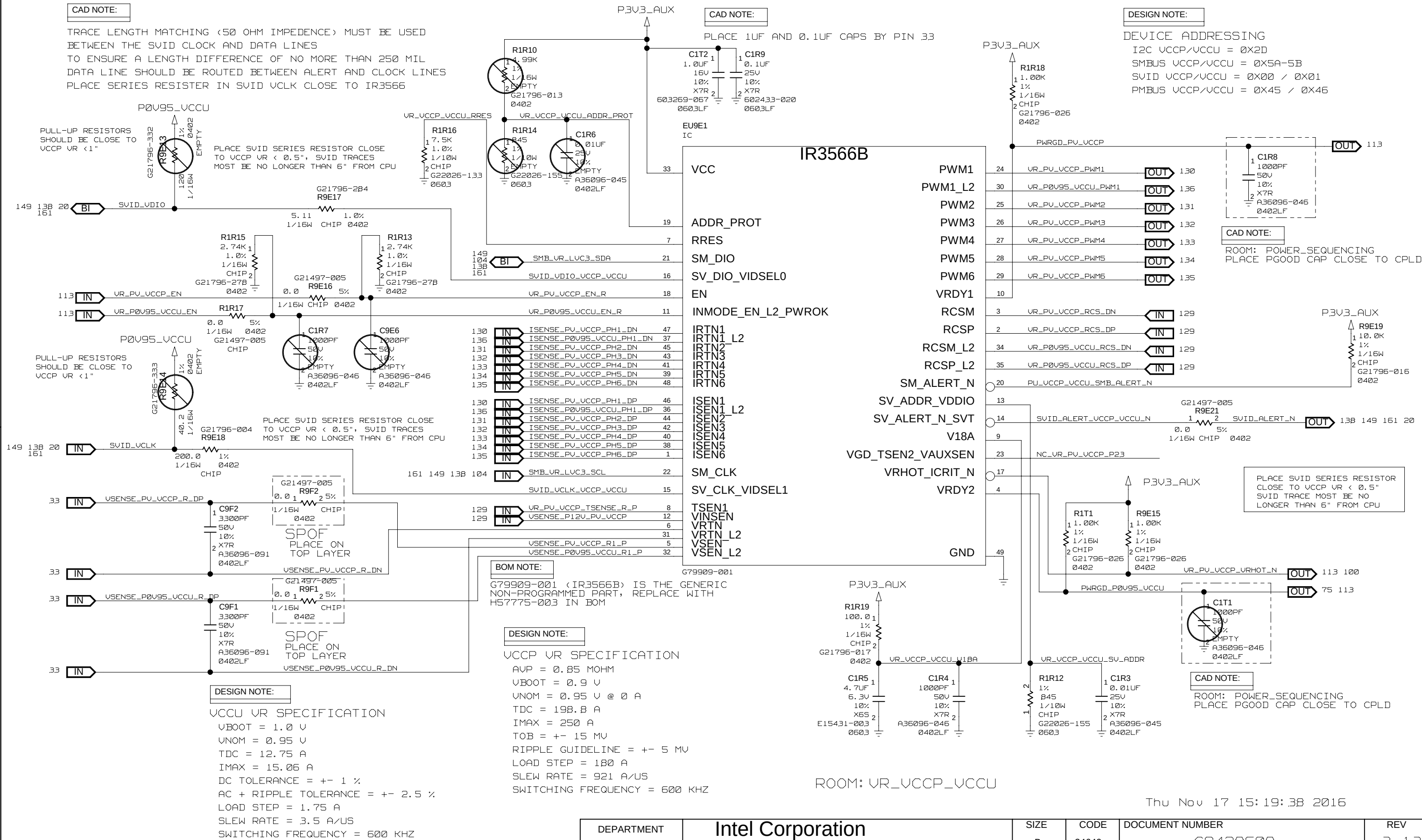
DO NOT SCALE DRAWING

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CAD NOTE:

TRACE LENGTH MATCHING (<50 OHM IMPEDENCE) MUST BE USED
BETWEEN THE SVID CLOCK AND DATA LINES
TO ENSURE A LENGTH DIFFERENCE OF NO MORE THAN 250 MIL
DATA LINE SHOULD BE ROUTED BETWEEN ALERT AND CLOCK LINES
PLACE SERIES RESISTOR IN SVID VCLK CLOSE TO IR3566



DESIGN NOTE:

VCCU VR SPECIFICATION

V_{BOOT} = 1.0 V
V_{NOM} = 0.95 V
TDC = 12.75 A
I_{MAX} = 15.06 A
DC TOLERANCE = + - 1 %
AC + RIPPLE TOLERANCE = + - 2.5 %
LOAD STEP = 1.75 A
SLEW RATE = 3.5 A/US
SWITCHING FREQUENCY = 600 KHZ

BOM NOTE:

G79909-001 (IR3566B) IS THE GENERIC
NON-PROGRAMMED PART, REPLACE WITH
H57775-003 IN BOM

DESIGN NOTE:

VCCP VR SPECIFICATION

AUP = 0.85 MOHM
VBOOT = 0.9 V
VNOM = 0.95 V @ 0 A
TDC = 198.8 A
IMAX = 250 A
TOB = +- 15 MV
RIPPLE GUIDELINE = +- 5 MV
LOAD STEP = 180 A
SLEW RATE = 921 A/US
SWITCHING FREQUENCY = 600 KHZ

CAD NOTE:

PLACE 1UF AND 0.1UF CAPS BY PIN 33

DESIGN NOTE:

DEVICE ADDRESSING

```
I2C VCCP/VCCU = 0X2D
SMBUS VCCP/VCCU = 0X5A-5B
SVID VCCP/VCCU = 0X00 / 0X01
PMBUS VCCP/VCCU = 0X45 / 0X46
```

CAD NOTE:

ROOM: POWER_SEQUENCING
PLACE PGOOD CAP CLOSE TO CPLD

PLACE SVID SERIES RESISTOR
CLOSE TO VCCP VR < 0.5"
SVID TRACE MUST BE NO
LONGER THAN 6" FROM CPU

CAD NOTE:

ROOM: POWER_SEQUENCING
PLACE PG00D CAP CLOSE TO CPLD

PV_VCCP/P0V95_VCCU CONTROLLER

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SCALE:

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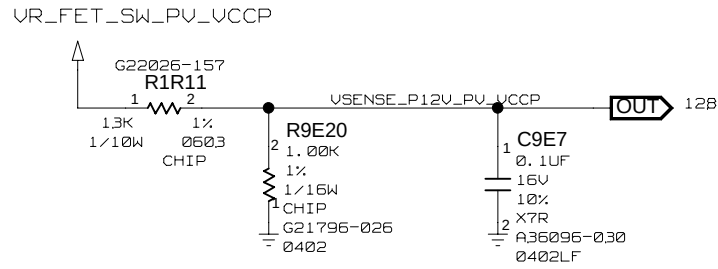
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1

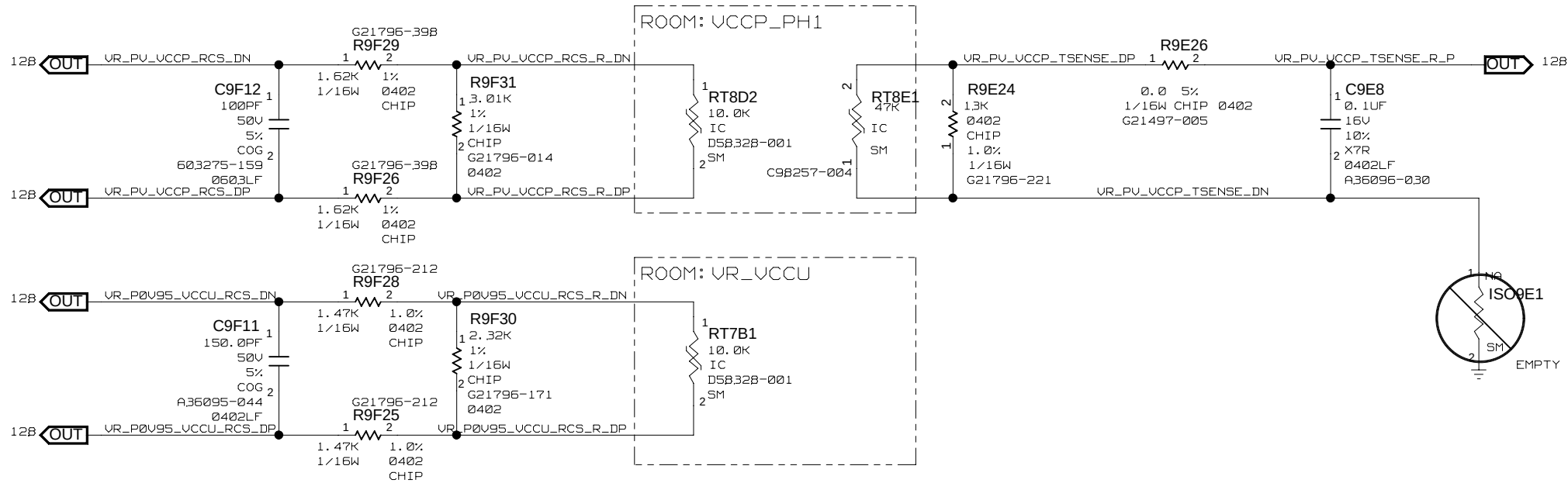
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CAD NOTE:

PLACE THERMISTORS ON TOP.
RCS THERMISTORS NEAR PHASE 1 INDUCTOR OF CORRESPONDING VR (VCCP OR VCCU)
TSENSE THERMISTOR, NEAR PHASE 1 DRIVER-FET OF VCCP VR
PLACE THE OTHER COMPONENTS NEAR CONTROLLER
ROUTE RCS AND TSENSE LINES AS DIFF PAIR BACK TO THE CONTROLLER



ROOM: VR_VCCP_VCCU

PV_VCCP/P0V95_VCCU TEMP COMPENSATION

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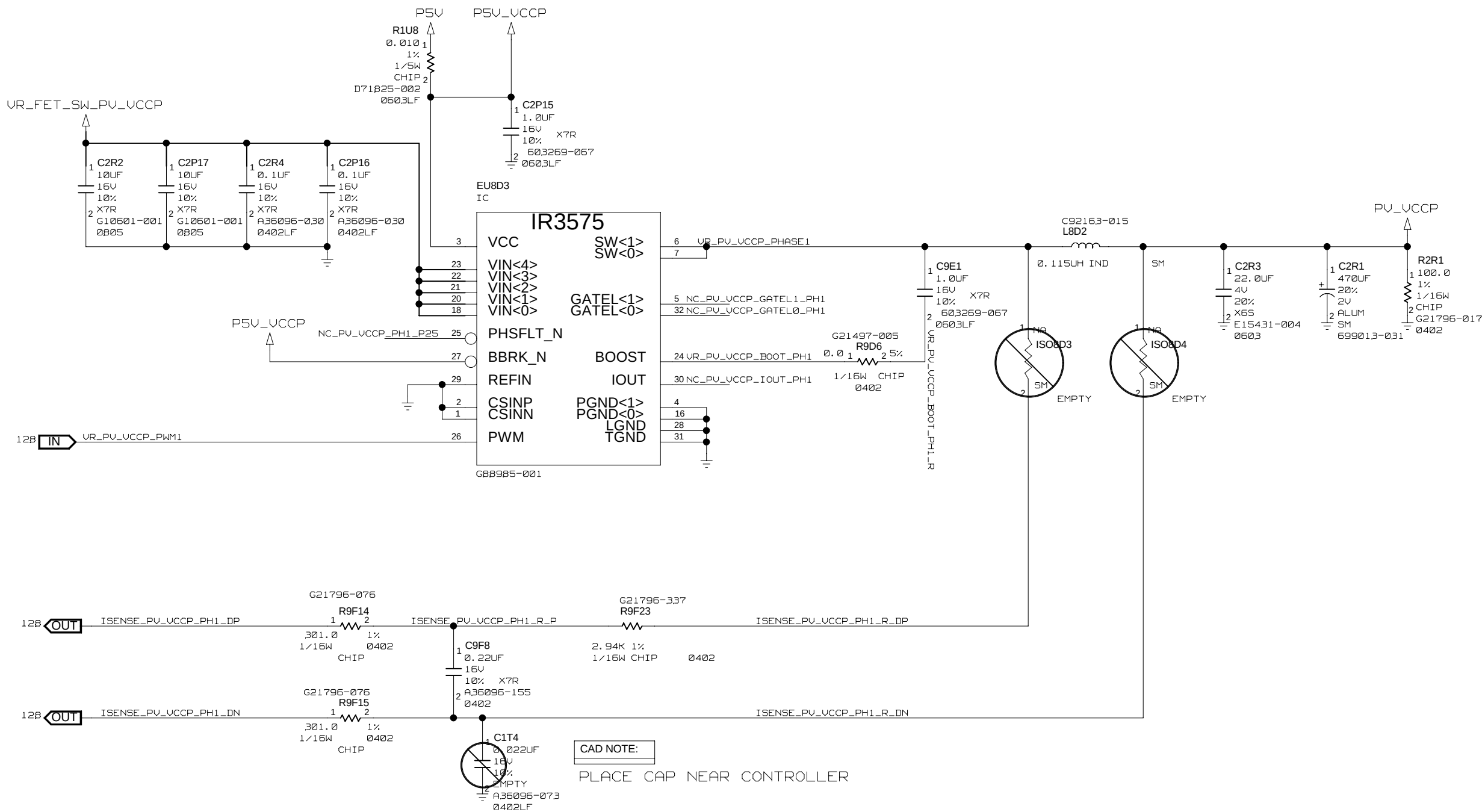
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SCALE:

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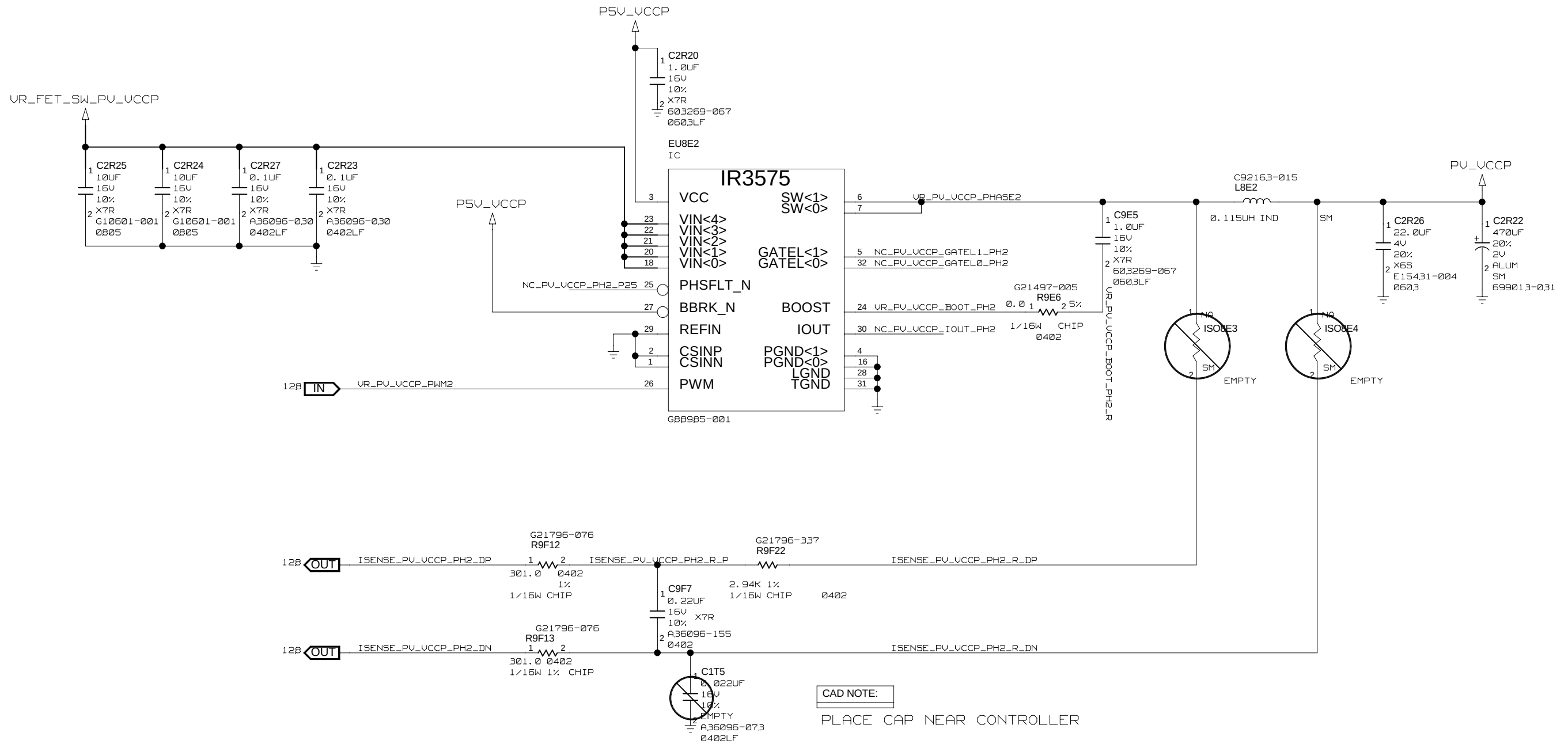
ROOM: VCCP_PH1

PV_VCCP PHASE 1

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		SCALE:		DO NOT SCALE DRAWING	SHEET 130 OF 167

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ROOM: VCCP_PH2

PV_VCCP PHASE 2

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CODE
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DOCUMENT NUMBER
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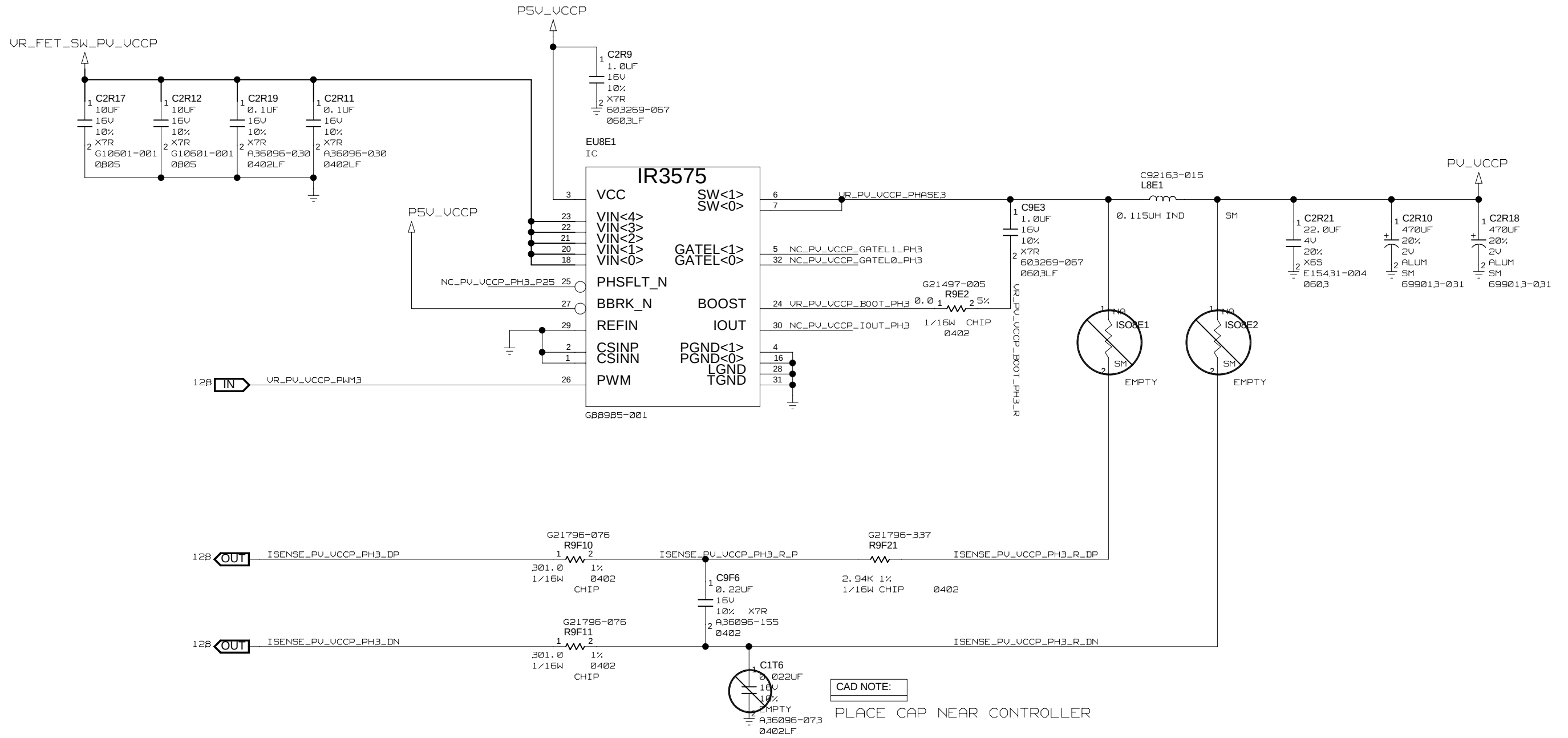
REV
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SCALE:

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ROOM: VCCP_PH3

PV_VCCP PHASE 3

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SIZE
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CODE
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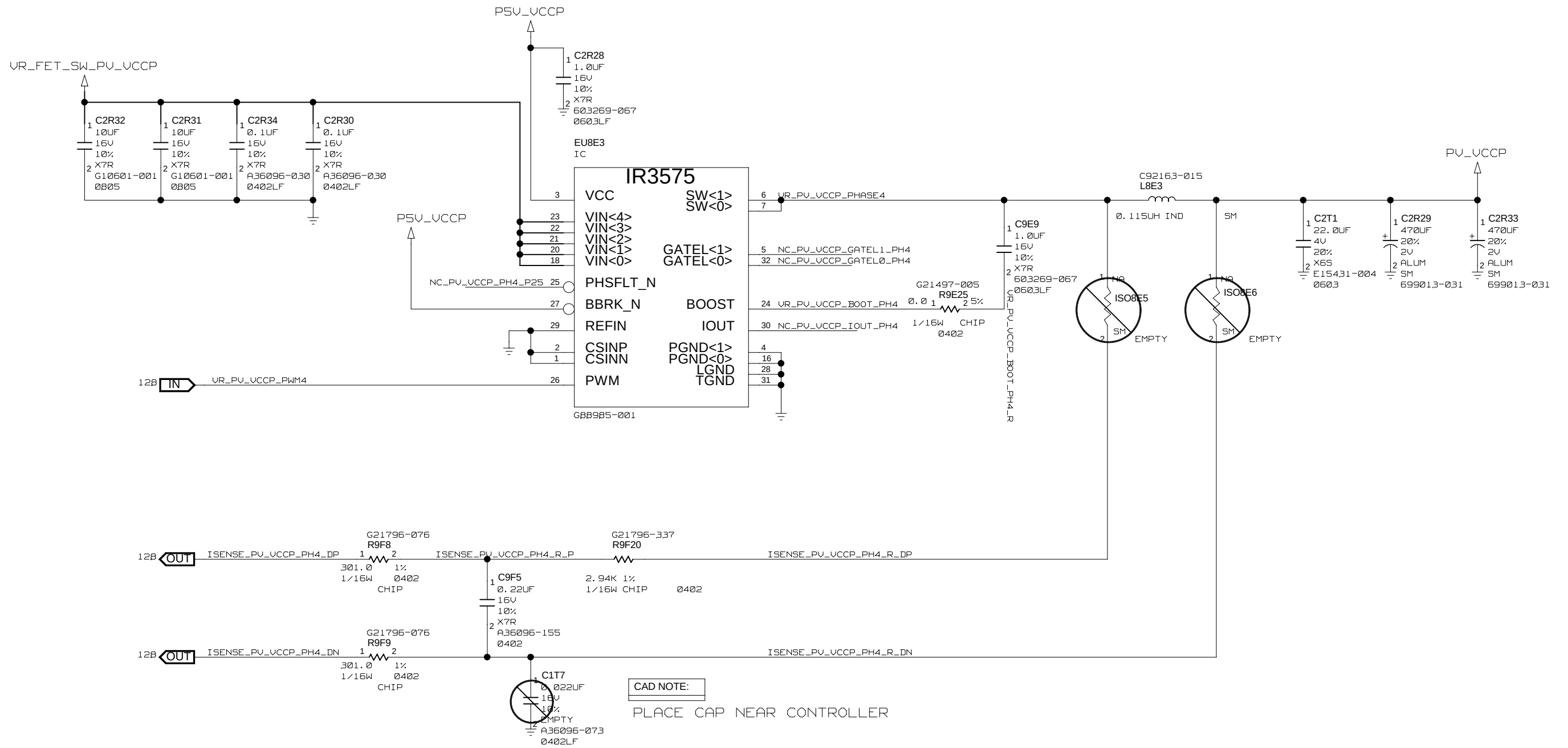
DOCUMENT NUMBER
G9428608

REV
.3.1.3

SCALE:

DO NOT SCALE DRAWING

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ROOM: VCCP_PH4

PV_VCCP PHASE 4

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CODE
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DOCUMENT NUMBER
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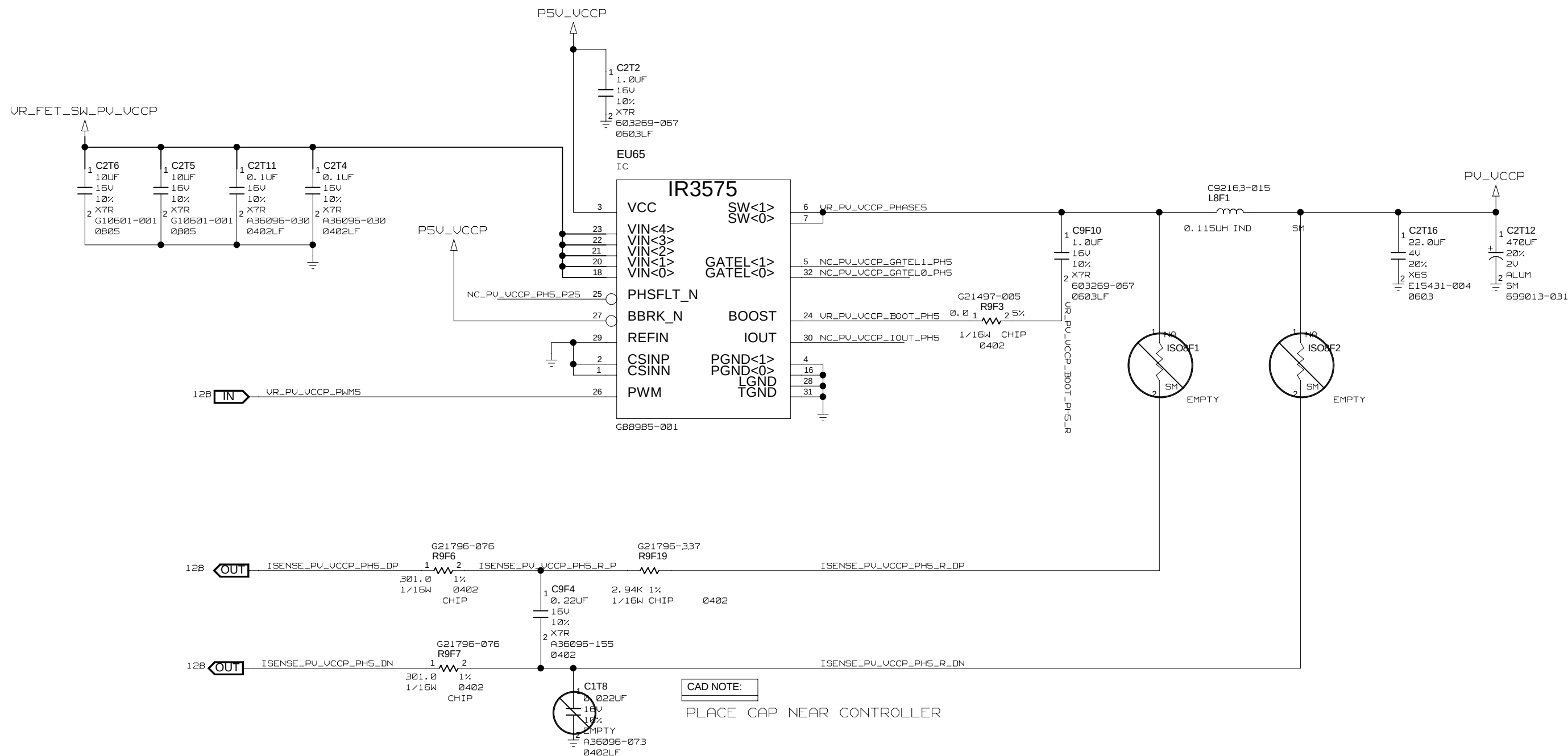
REV
.3.1.3

SCALE:

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ROOM: VCCP_PHS

PV_VCCP PHASE 5

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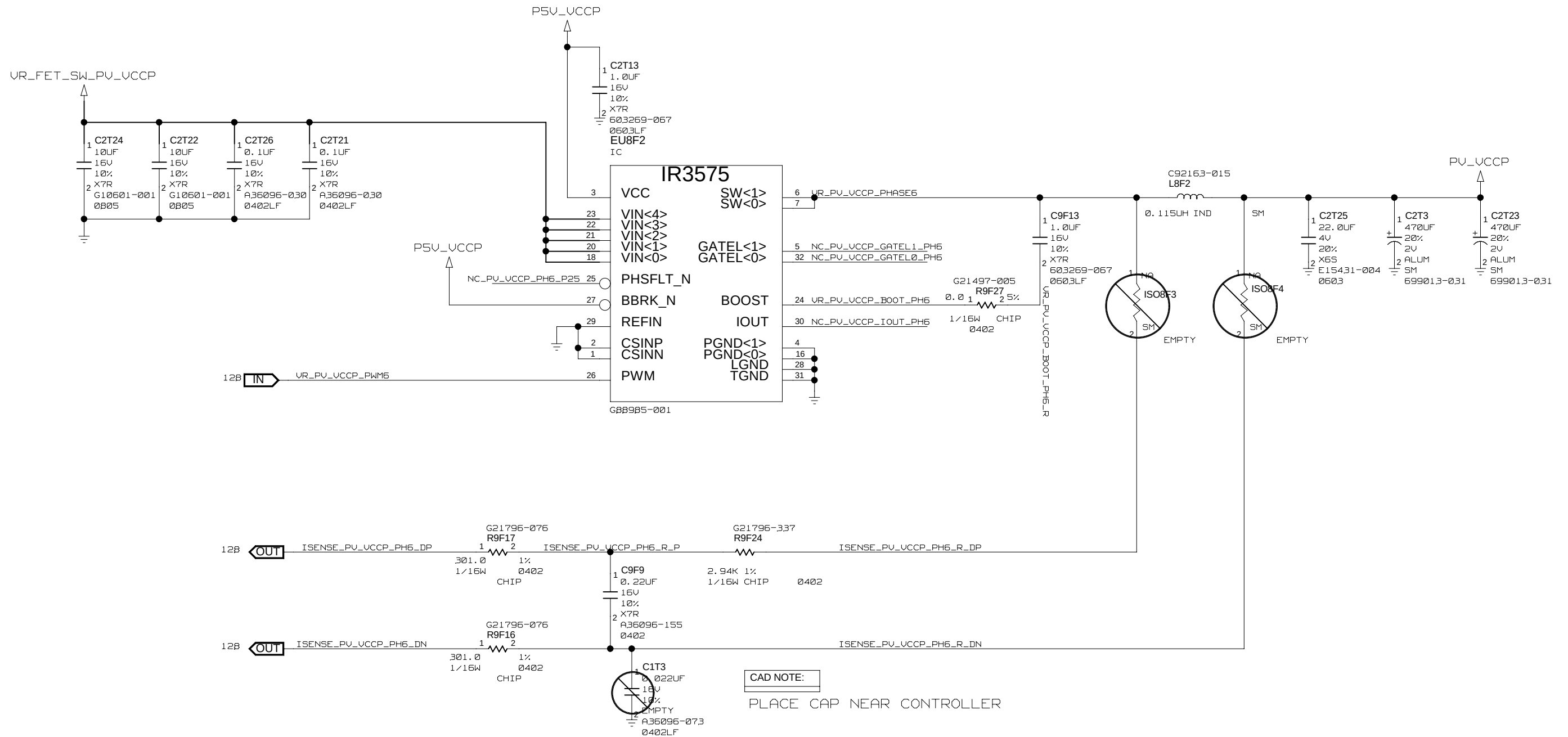
REV

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SCALE:

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CAD NOTE:

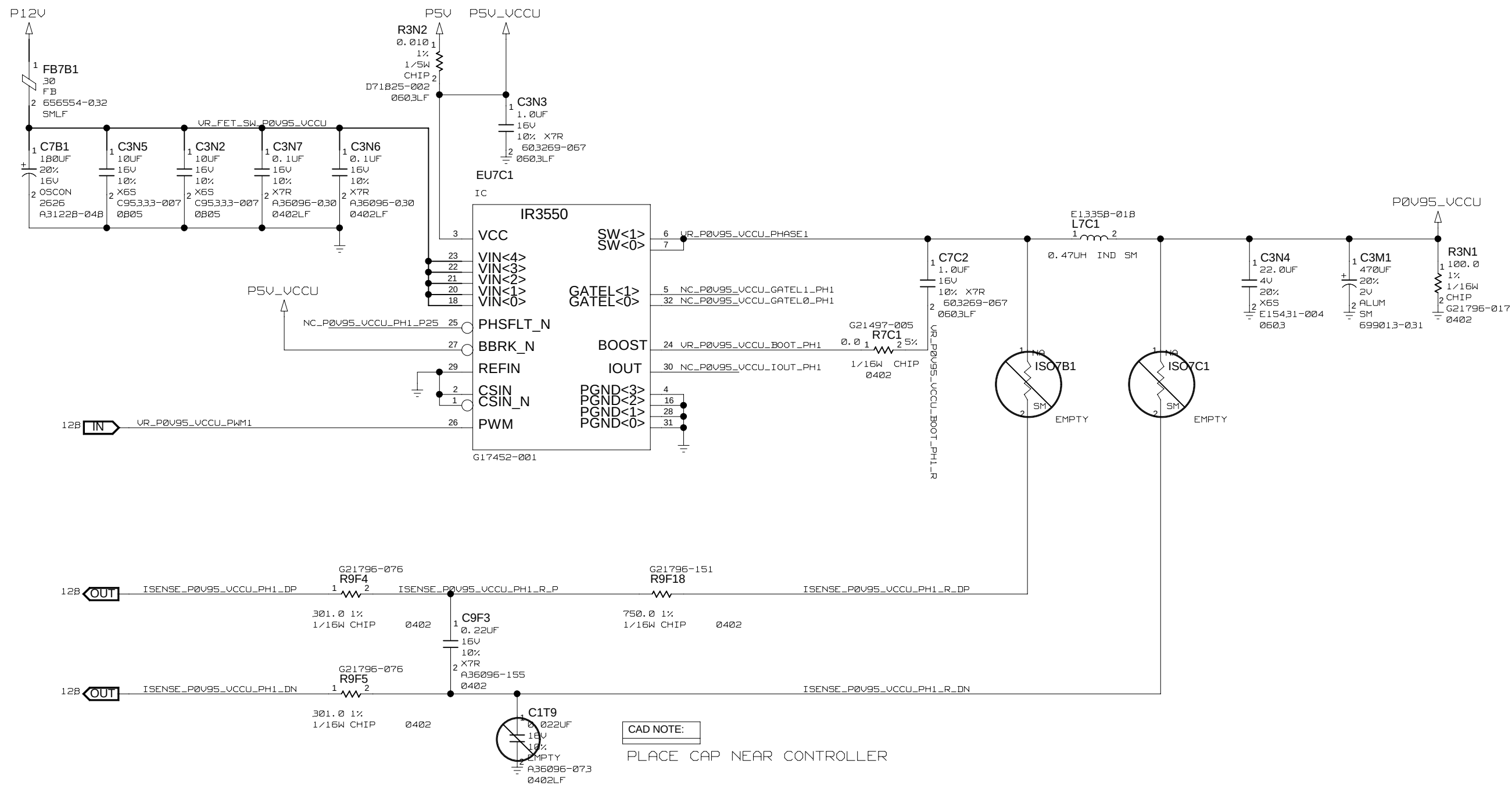
PLACE CAP NEAR CONTROLLER

ROOM: VCCP_PH6

PV_VCCP PHASE 6

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DEPARTMENT	Intel Corporation 2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119	SIZE	CODE	DOCUMENT NUMBER		REV
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		SCALE:		DO NOT SCALE DRAWING		SHEET 135 OF 167



ROOM: VCCU_PH1

P0V95_VCCU PHASE 1

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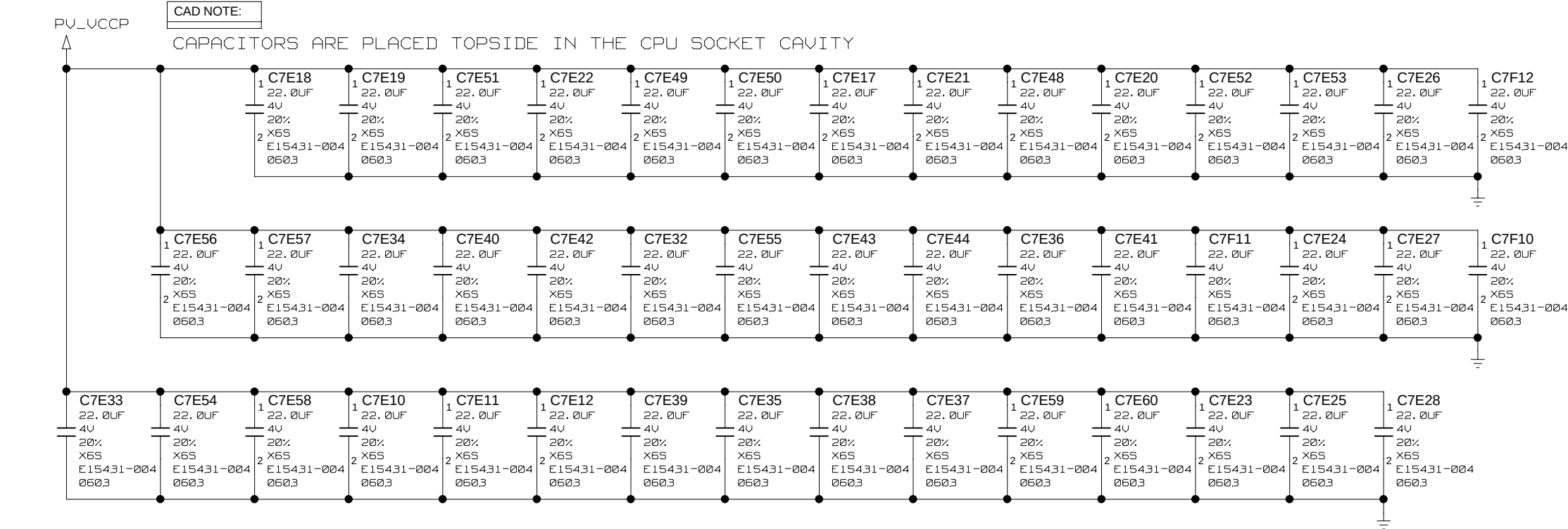
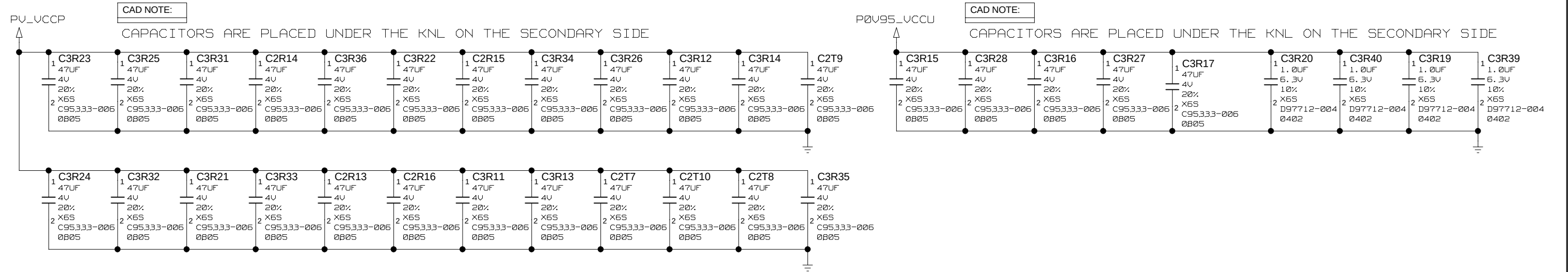
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SCALE:

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ROOM: KNL

PV_VCCP/P0V95_VCCU DECOUPLING

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		SCALE:		DO NOT SCALE DRAWING	SHEET 137 OF 167

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CAD NOTE:

TRACE LENGTH MATCHING MUST BE USED BETWEEN THE CLOCK AND DATA LINES
TO ENSURE A LENGTH DIFFERENCE OF NO MORE THAN 250 MIL
DATA LINE SHOULD BE ROUTED BETWEEN ALERT AND CLOCK LINES

DESIGN NOTE:

VCCCLR VR SPECIFICATION

AVP = 1.8 MOHM
VBOOT = 0.9 V
UNOM = 0.845 V @ 0 A
TDC = 50.68 A
IMAX = 69.00 A
DC TOLERANCE = $\pm 1\%$
AC + RIPPLE TOLERANCE = $\pm 2.7\%$
LOAD STEP = 43 A
SLEW RATE = 131.8 A/US
SWITCHING FREQUENCY = 600 KHZ

DESIGN NOTE:

VCCMLB VR SPECIFICATION

VBOOT = 0.9 V
UNOM = 0.95 V
TDC = 73.96 A
IMAX = 91.73 A
DC TOLERANCE = $\pm 1\%$
AC + RIPPLE TOLERANCE = ± 40 MV
LOAD STEP = 25.3 A
SLEW RATE = 77 A/US
SWITCHING FREQUENCY = 600 KHZ

DESIGN NOTE:

DEVICE ADDRESSING

I2C VCCCLR/VCCMLB = 0X33
SMBUS VCCCLR/VCCMLB = 0X66-67
SUID VCCCLR/VCCMLB = 0X06 / 0X07
PMBUS VCCCLR/VCCMLB = 0X73 / 0X74

CAD NOTE:

ROOM: POWER_SEQUENCING
PLACE PGOOD CAP CLOSE TO CPLD

PLACE SUID_ALERT SERIES RESISTOR
CLOSE TO VCCCLR VR < 0.5"
SUID TRACE MOST BE NO LONGER
THAN 6" FROM VCCD345 VR

CAD NOTE:

ROOM: POWER_SEQUENCING
PLACE PGOOD CAP CLOSE TO CPLD

PLACE SUID_SERIES RESISTOR
CLOSE TO VCCCLR VR < 0.5"
SUID TRACES MOST BE NO
LONGER THAN 6" FROM VCCD345 VR

BOM NOTE:

G79911-001 (IR3570B) IS THE GENERIC
NON-PROGRAMMED PART, REPLACE WITH
H59368-004 IN BOM

ROOM: VR_VCCCLR/VCCMLB

P0V75_VCCCLR/P0V95_VCCMLB CONTROLLER

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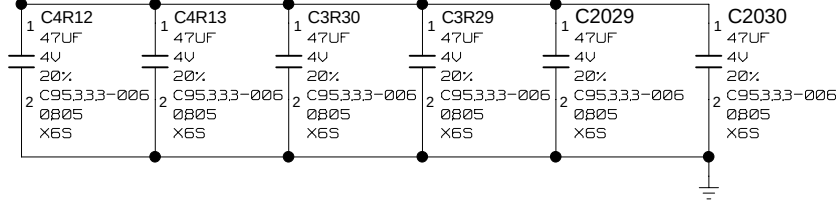
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P0V75_VCCCLR

CAD NOTE:

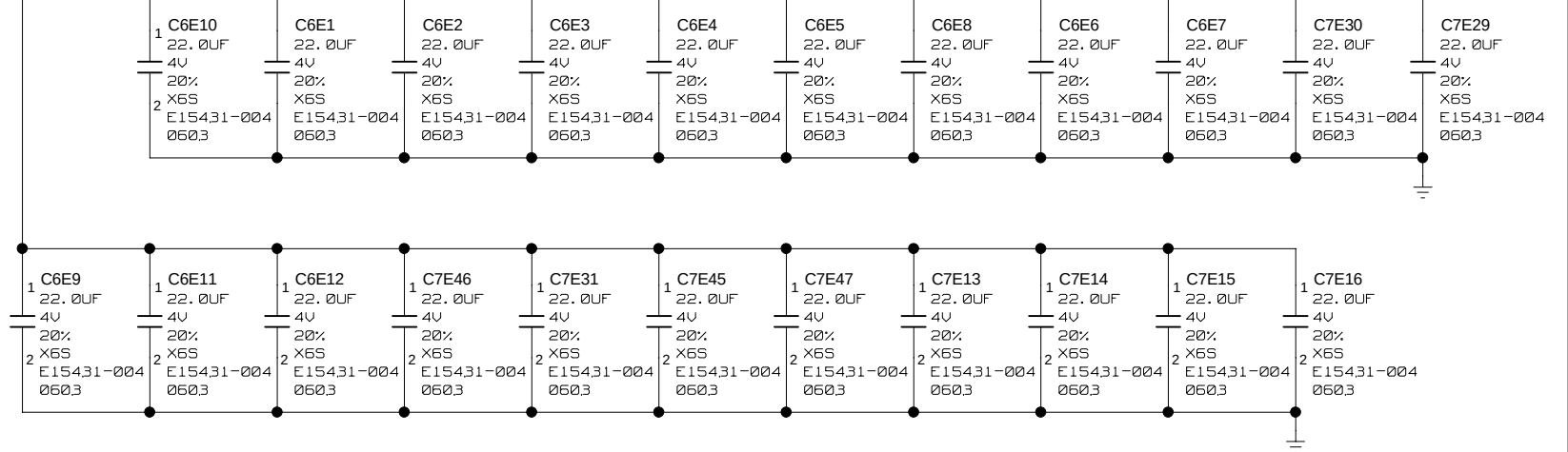
CAPACITORS ARE PLACED UNDER THE KNL ON THE SECONDARY SIDE



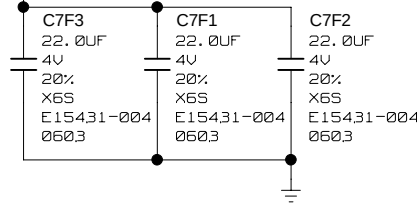
P0V75_VCCCLR

CAD NOTE:

CAPACITORS ARE PLACED TOPSIDE IN THE CPU SOCKET CAVITY



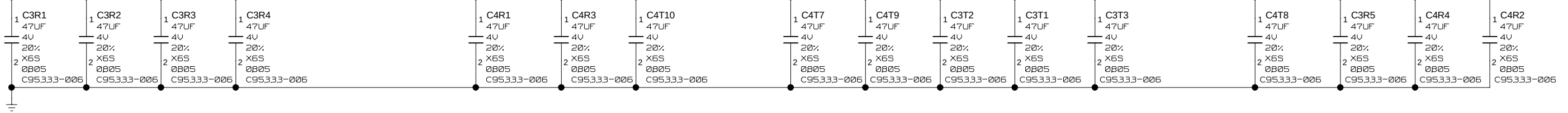
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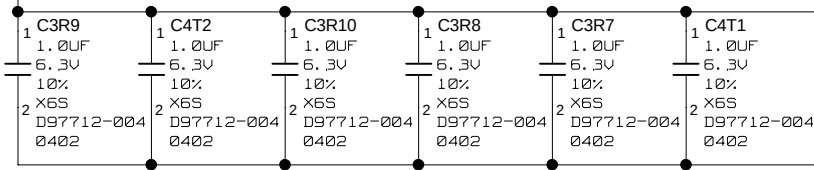
P0V95_VCCMLB

CAD NOTE:

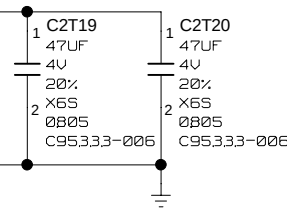
CAPACITORS ARE PLACED UNDER THE KNL ON THE SECONDARY SIDE



P0V95_VCCMLB



ADDED FOR EPD STUDY



ROOM: KNL

P0V75_VCCCLR/P0V95_VCCMLB DECOUPLING

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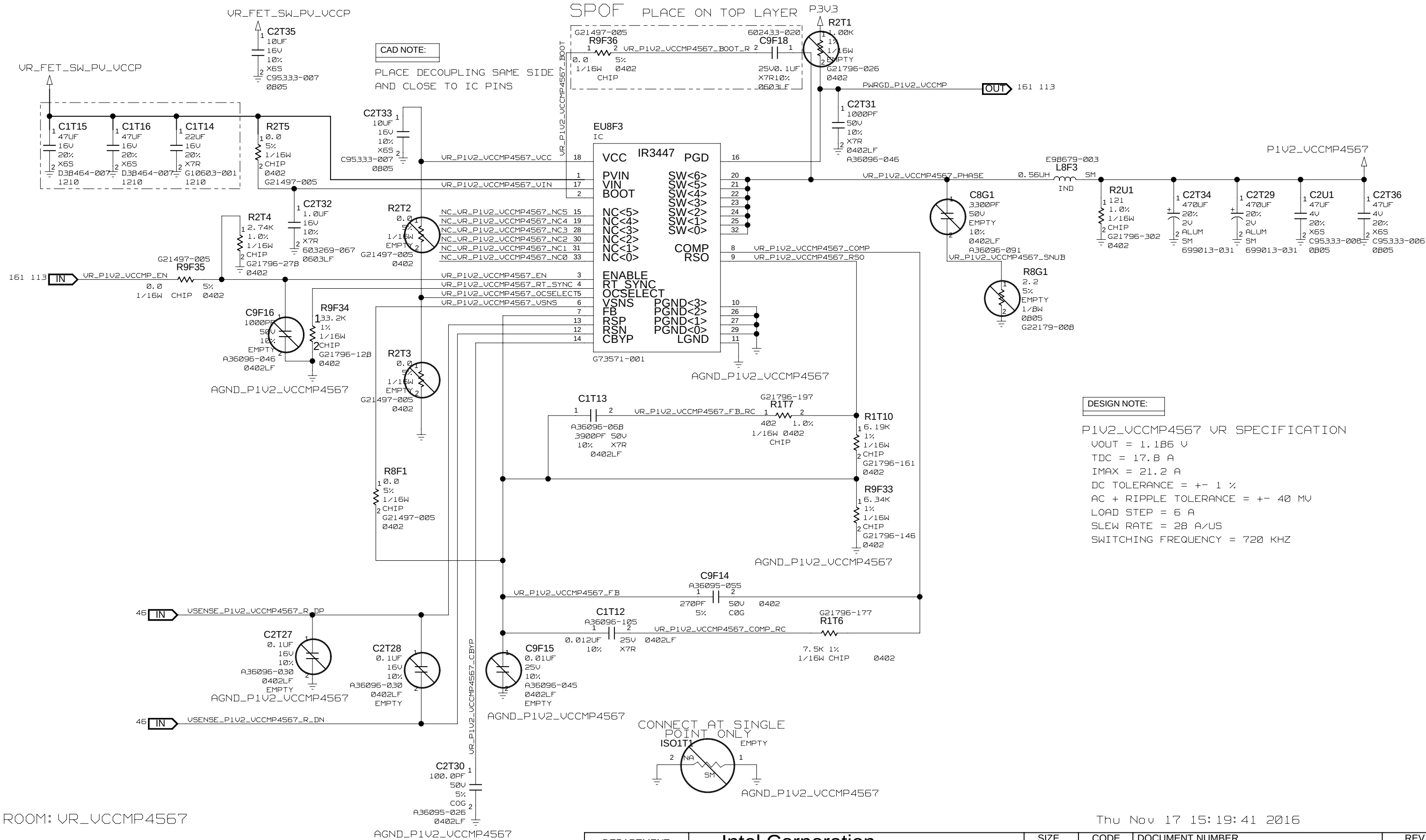
DO NOT SCALE DRAWING

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CAD NOTE:

TRACE LENGTH MATCHING MUST BE USED BETWEEN THE CLOCK AND DATA LINES
TO ENSURE A LENGTH DIFFERENCE OF NO MORE THAN 250 MIL
DATA LINE SHOULD BE ROUTED BETWEEN ALERT AND CLOCK LINES

DESIGN NOTE:

VCCD012 VR SPECIFICATION
VB00T = 1.21 V
VNOM = 1.21 V
TDC = 35.6 A
IMAX = 38.9 A
DC TOLERANCE = $\pm 0.5\%$
AC + RIPPLE TOLERANCE = ± 38 MV
LOAD STEP = 31.03 A
SLEW RATE = 12.3 A/US
SWITCHING FREQUENCY = 600 KHZ

DESIGN NOTE:

VCCD345 VR SPECIFICATION
VB00T = 1.21 V
VNOM = 1.21 V
TDC = 35.6 A
IMAX = 38.9 A
DC TOLERANCE = $\pm 0.5\%$
AC + RIPPLE TOLERANCE = ± 38 MV
LOAD STEP = 31.03 A
SLEW RATE = 12.3 A/US
SWITCHING FREQUENCY = 600 KHZ

DESIGN NOTE:

DEVICE ADDRESSING

I2C VCCD012/VCCD345 = 0X36
SMBUS VCCD012/VCCD345 = 0X6C-6D
SVID VCCD012/VCCD345 = 0X02 / 0X04
PMBUS VCCD012/VCCD345 = 0X77 / 0X76

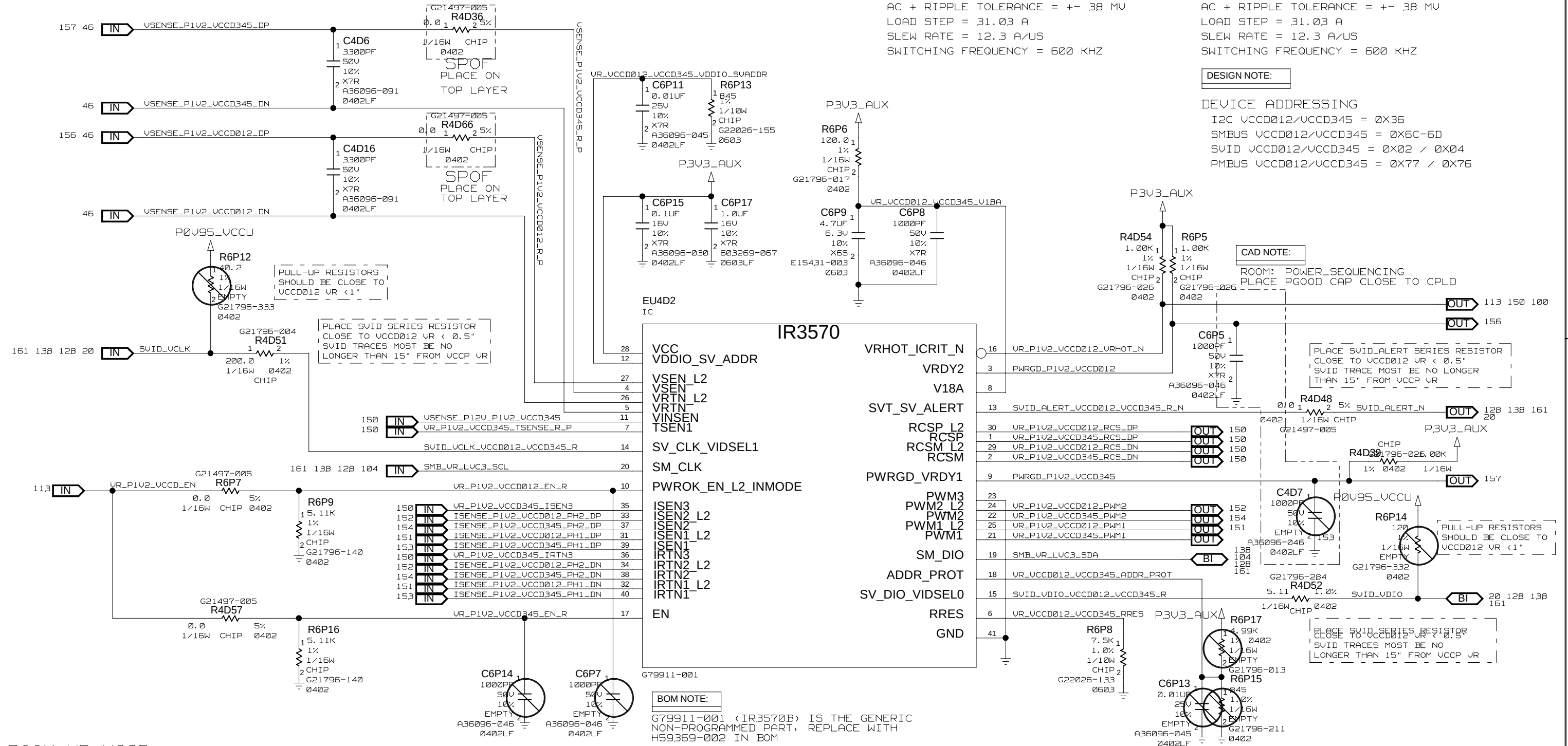
CAD NOTE:

ROOM: POWER_SEQUENCING
PLACE PG00D CAP CLOSE TO CPLD

PLACE SVID_ALERT SERIES RESISTOR
CLOSE TO VCCD012 VR < 0.5"
SVID TRACE MUST BE NO LONGER
THAN 15" FROM UCCP VR

PULL-UP RESISTORS
SHOULD BE CLOSE TO
VCCD012 VR < 1"

PLACE SVID_ALERT SERIES RESISTOR
CLOSE TO VCCD012 VR < 0.5"
SVID TRACES MUST BE NO
LONGER THAN 15" FROM UCCP VR



ROOM: VR_VCCD

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P1V2_VCCD012/P1V2_VCCD345 CONTROLLER

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CODE

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REV

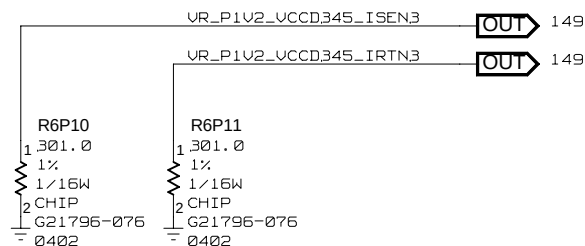
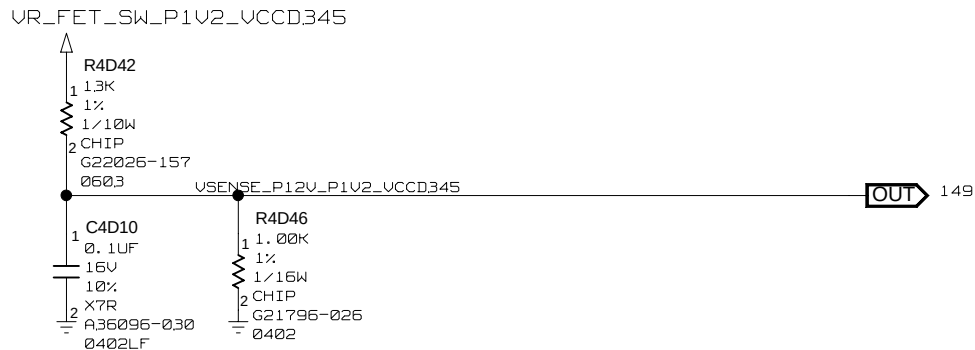
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SCALE:

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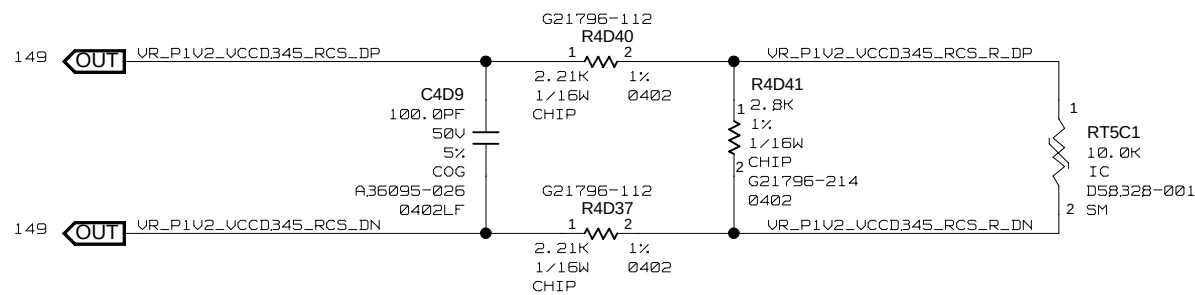
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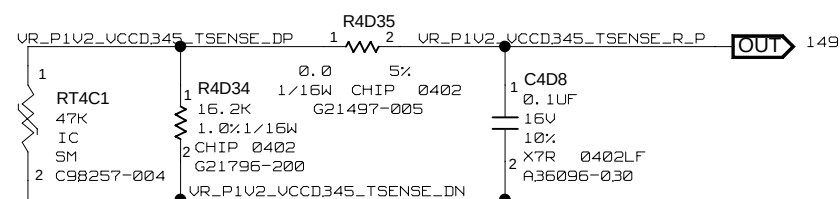
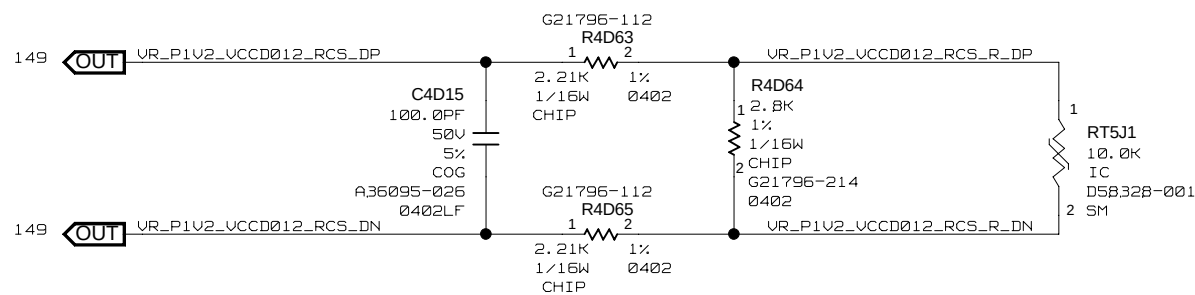
CAD NOTE:

PLACE THERMISTOR ON TOP, NEAR PHASE 1 INDUCTOR
PLACE THE OTHER COMPONENTS NEAR CONTROLLER
ROUTE RCS LINES AS DIFF PAIR



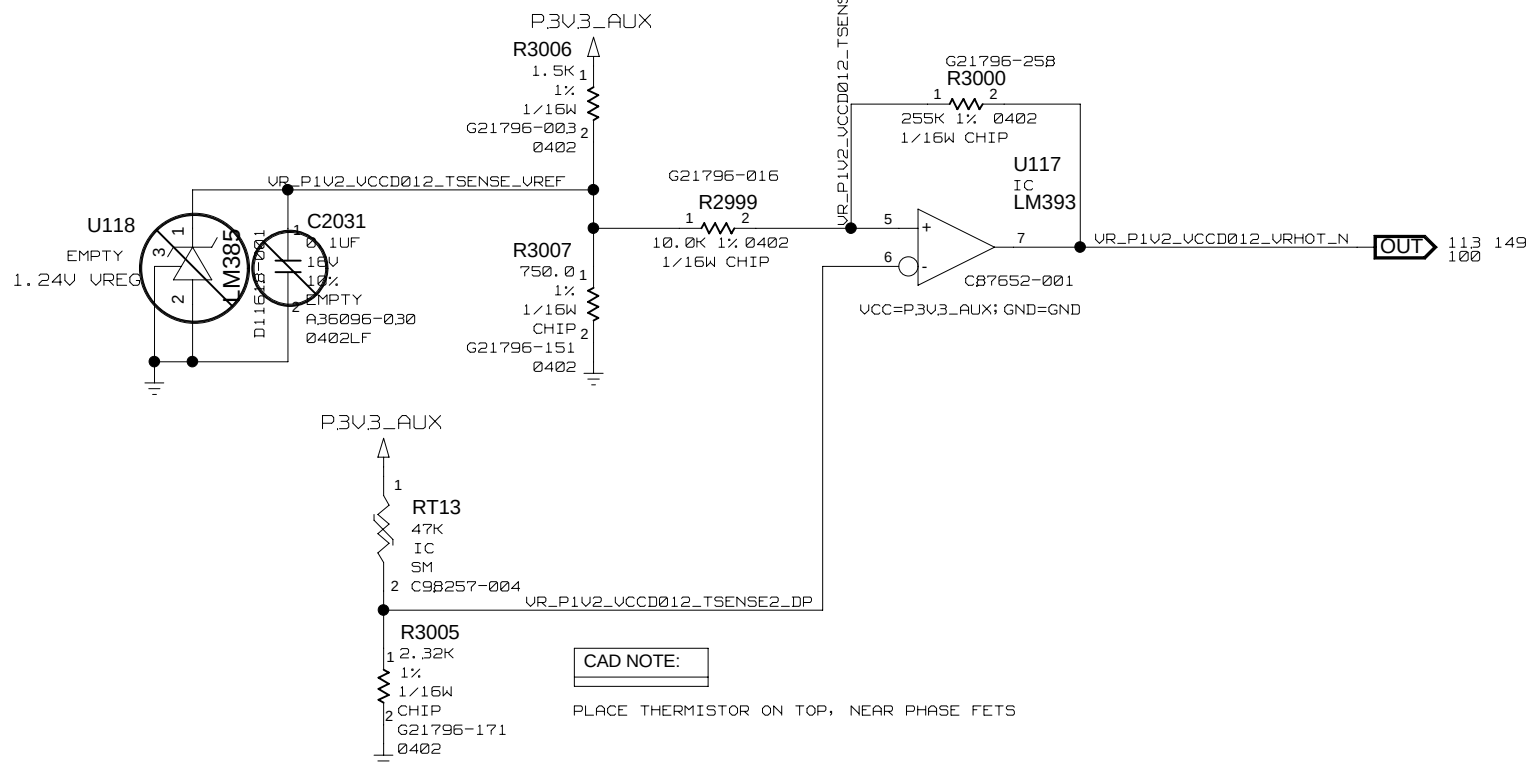
CAD NOTE:

PLACE THERMISTOR ON TOP, NEAR PHASE 1 INDUCTOR
PLACE THE OTHER COMPONENTS NEAR CONTROLLER
ROUTE RCS LINES AS DIFF PAIR



CAD NOTE:

PLACE THERMISTOR ON TOP, NEAR PHASE 1 FETS
PLACE THE OTHER COMPONENTS NEAR CONTROLLER
ROUTE TSENSE LINES AS DIFF PAIR



CAD NOTE:

PLACE THERMISTOR ON TOP, NEAR PHASE FETS

ROOM: VR_VCCD

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P1V2_VCCD TEMP COMPENSATION

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B

CODE
34649

DOCUMENT NUMBER
G9428608

REV
.3.1.3

SCALE:

DO NOT SCALE DRAWING

SHEET 150 OF 167



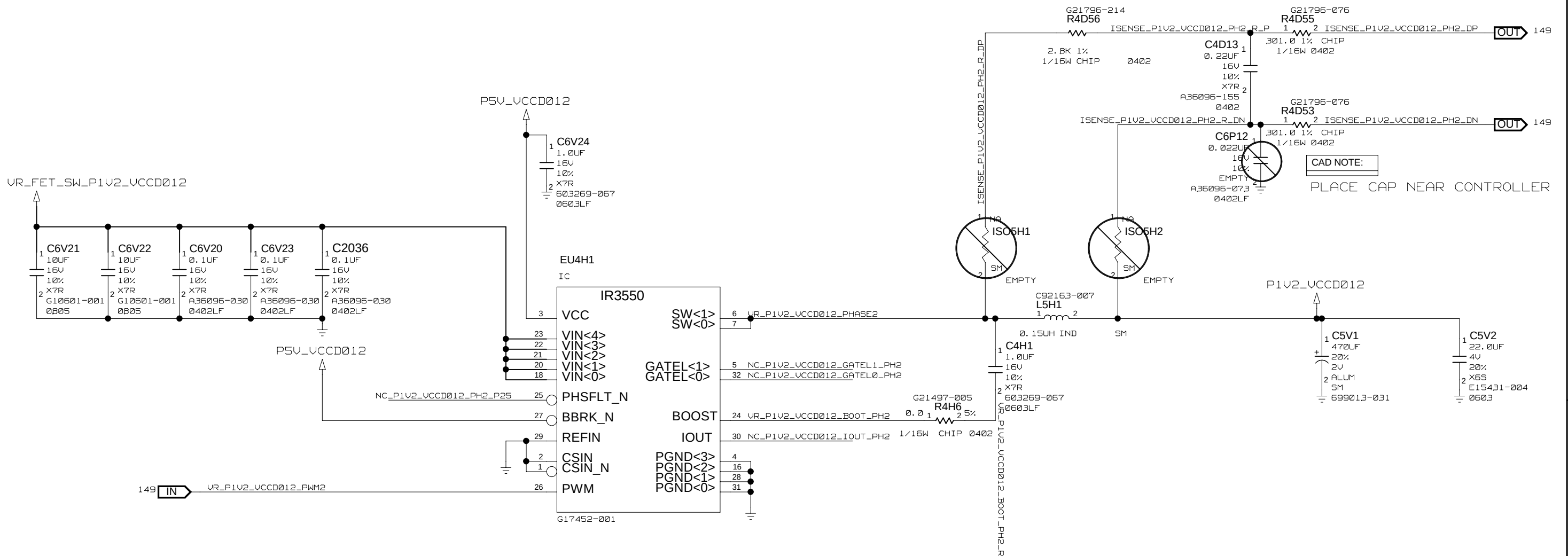
SHEET 151 OF 167

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ROOM: VCCD012_PH2

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P1V2_VCCD012 PHASE 2

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SCALE:		DO NOT SCALE DRAWING			SHEET 152 OF 167



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SHEET 15.3 OF 167



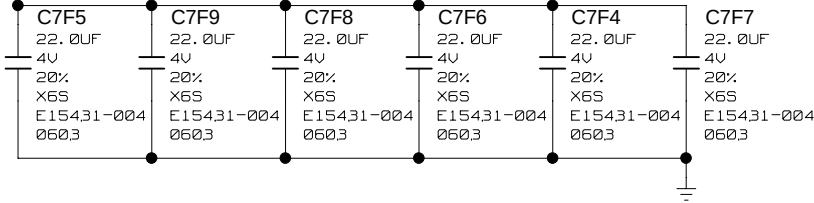
SHEET 154 OF 167

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P1V2_VCCD012

CAD NOTE:

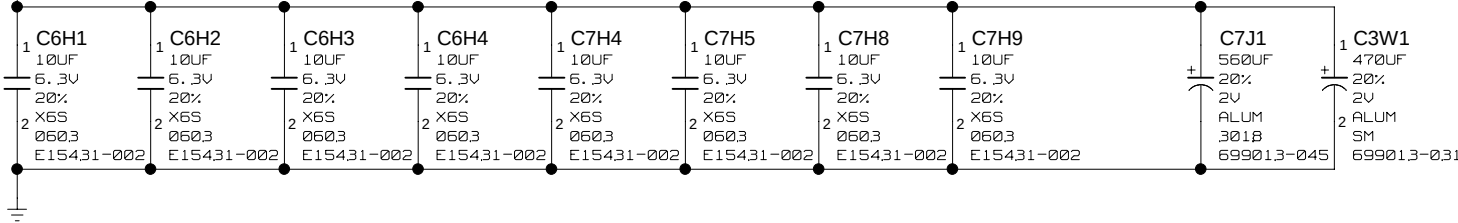
CAPACITORS ARE PLACED TOPSIDE IN THE CPU SOCKET CAVITY



P1V2_VCCD012

CAD NOTE:

PLACE CLOSE TO DDR4 DIMMS

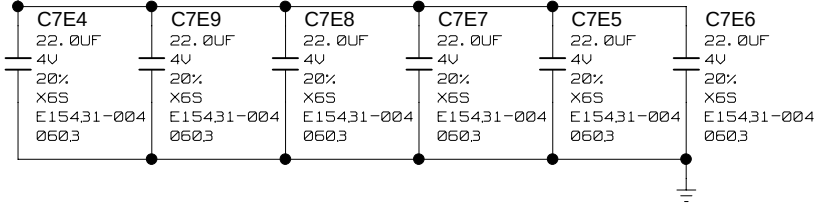


ROOM: DDR4_DIMM_0

P1V2_VCCD345

CAD NOTE:

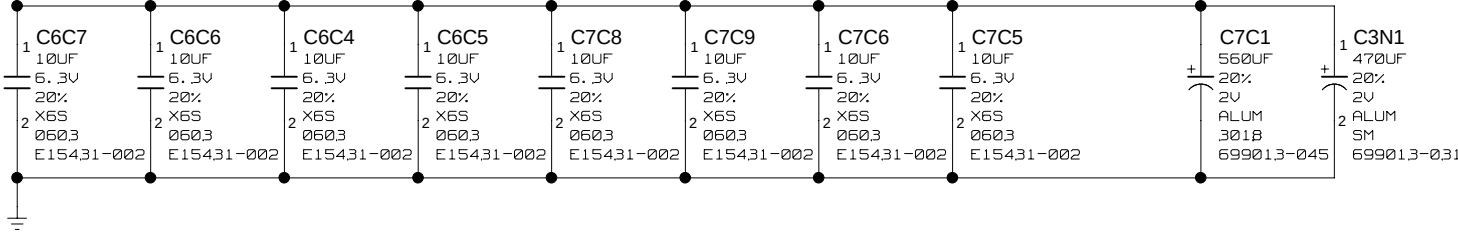
CAPACITORS ARE PLACED TOPSIDE IN THE CPU SOCKET CAVITY



P1V2_VCCD345

CAD NOTE:

PLACE CLOSE TO DDR4 DIMMS



ROOM: DDR4_DIMM_3

ROOM: KNL

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P1V2_VCCD012/VCCD.345 DECOUPLING

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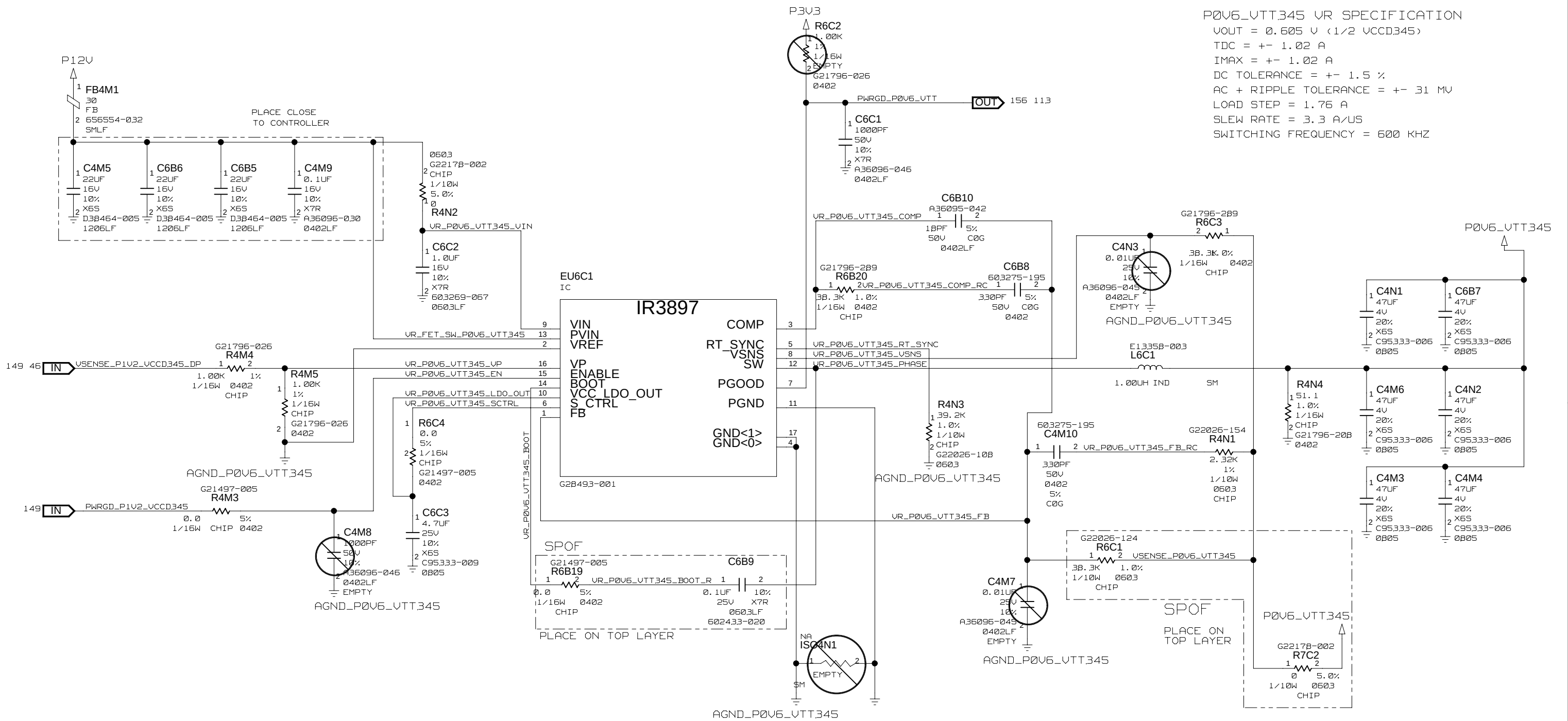
DOCUMENT NUMBER
G9428608

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ROOM: VR_VTT345

P0V6_VTT345 VR

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DOCUMENT NUMBER

G9428608

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SCALE:

DO NOT SCALE DRAWING

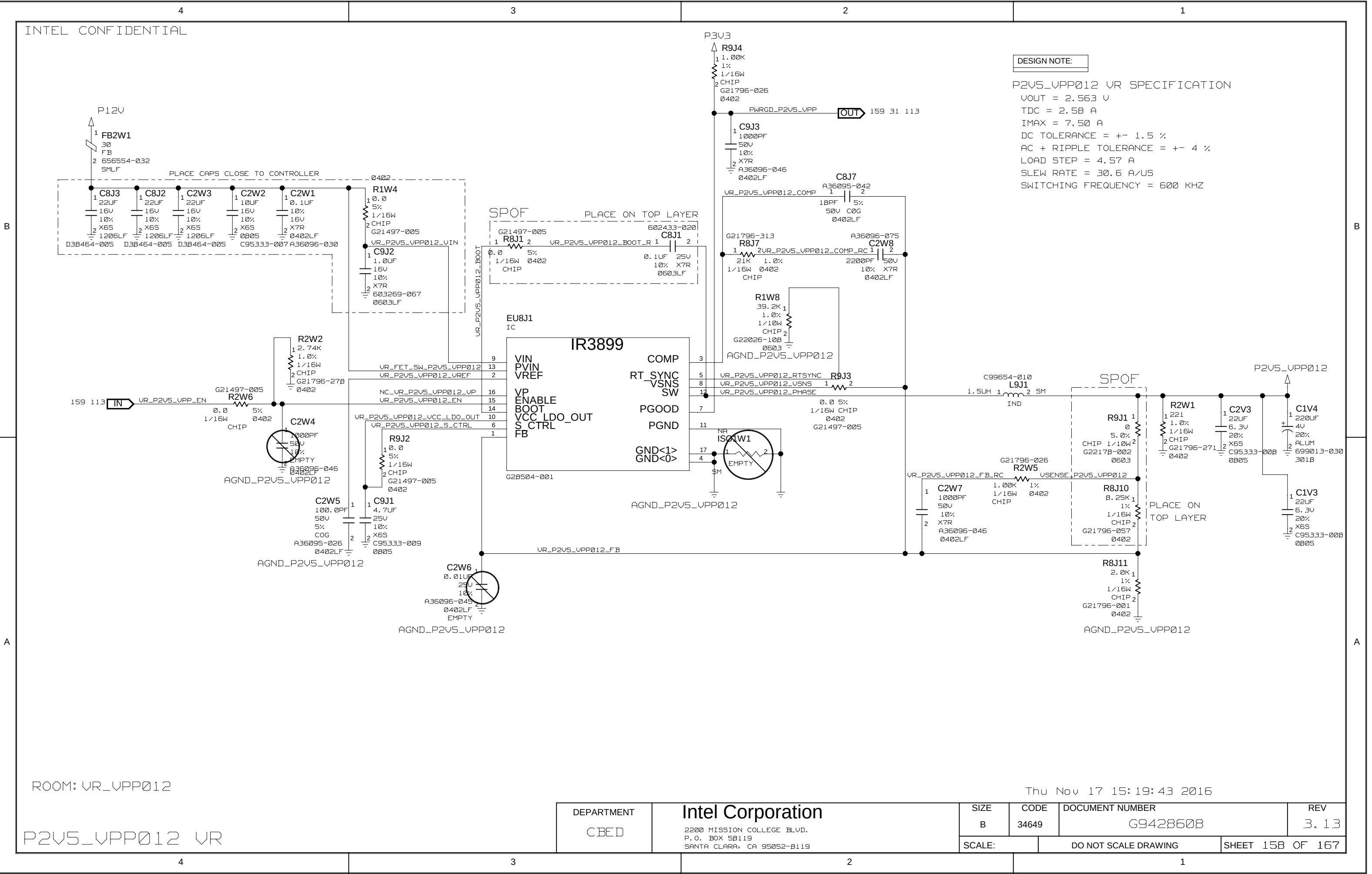
SHEET 157 OF 167

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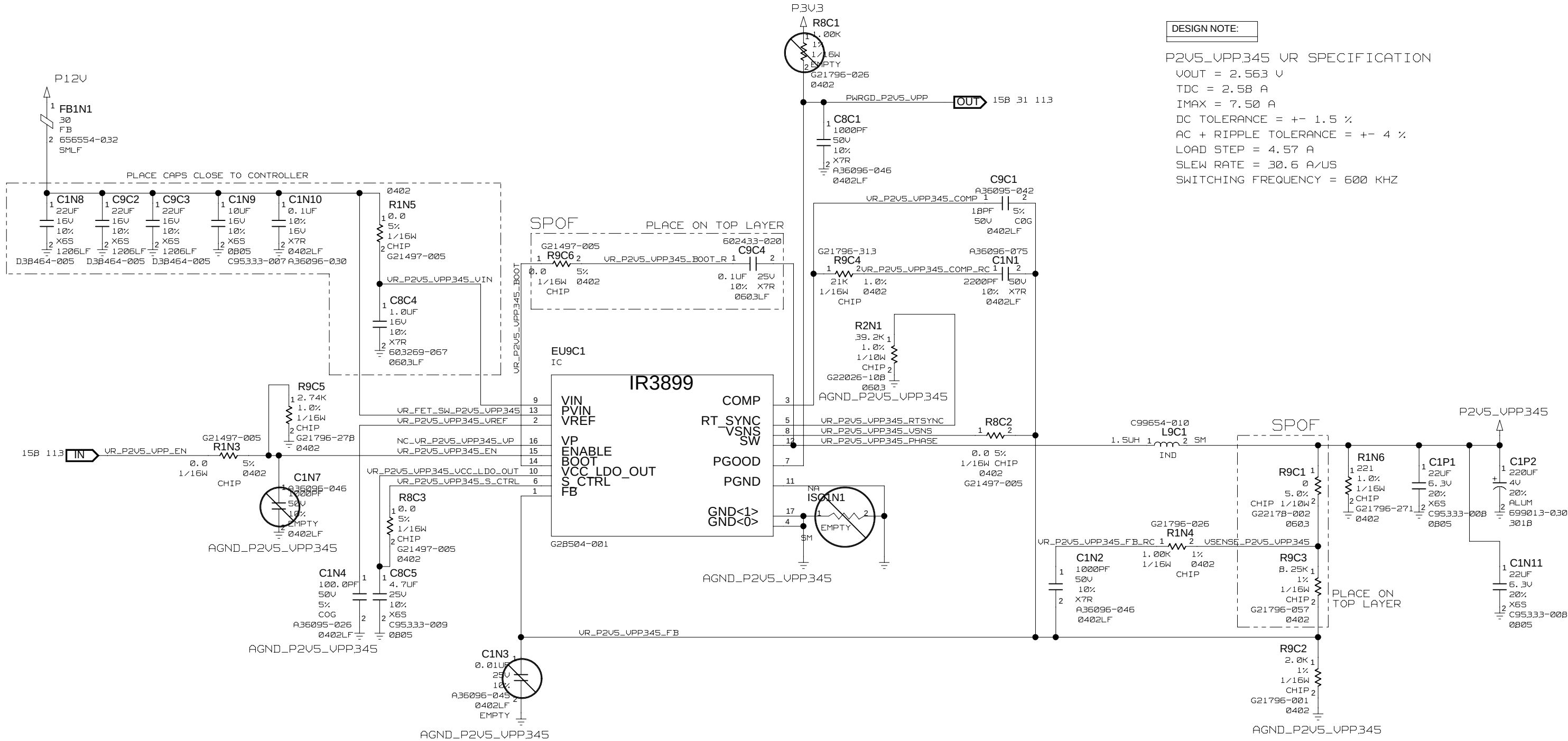


B

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ROOM: VR_VPP345

P2V5_VPP345 VR

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		SCALE:		DO NOT SCALE DRAWING	SHEET 159 OF 167	

CAD NOTE:

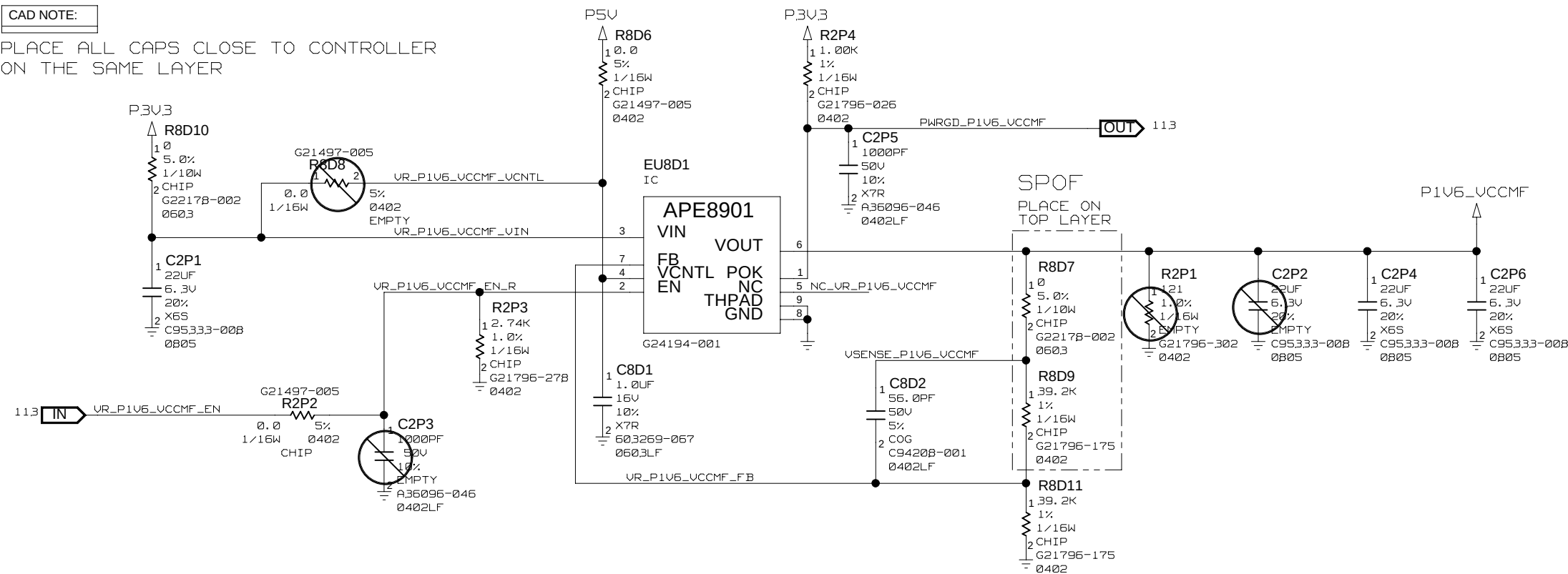
PLACE ALL CAPS CLOSE TO CONTROLLER
ON THE SAME LAYER

BOM NOTE:

REPLACE G24194-001 WITH H70171-001 IN BOM

DESIGN NOTE:

PIV6_VCCMF VR SPECIFICATION
VOUT = 1.6 V
TDC = 0.05 A
IMAX = 0.50 A
DC TOLERANCE = +- 1 %
AC + RIPPLE TOLERANCE = +- 2.8 %
LOAD STEP = 0.12 MA
SLEW RATE = 1 A/US
SWITCHING FREQUENCY = NA (LINEAR)



ROOM: VR_VCCMFUSE

PIV6_VCCMFUSE VR

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CAD NOTE:

TRACE LENGTH MATCHING MUST BE USED BETWEEN THE CLOCK AND DATA LINES
TO ENSURE A LENGTH DIFFERENCE OF NO MORE THAN 250 MIL
DATA LINE SHOULD BE ROUTED BETWEEN ALERT AND CLOCK LINES

DESIGN NOTE:

VCC_CDCORE VR SPECIFICATION

VB00T = 0.9 V
UNOM = 0.9 V
TDC = 8.89 A
IMAX = 9.86 A
DC TOLERANCE = $\pm 1.5\%$
AC + RIPPLE TOLERANCE = $\pm 4.5\%$
LOAD STEP = 2.2 A
SLEW RATE = 8.6 A/US
SWITCHING FREQUENCY = 600 KHZ

DESIGN NOTE:

VCCMP0123 VR SPECIFICATION

VB00T = 1.185 V
UNOM = 1.185 V
TDC = 17.8 A
IMAX = 21.2 A
DC TOLERANCE = $\pm 1\%$
AC + RIPPLE TOLERANCE = ± 40 MV
LOAD STEP = 6 A
SLEW RATE = 31 A/US
SWITCHING FREQUENCY = 720 KHZ

DESIGN NOTE:

DEVICE ADDRESSING

I2C VCC_CDCORE/VCCMP0123 = 0X2B
SMBUS VCC_CDCORE/VCCMP0123 = 0X56-57
SVID VCC_CDCORE/VCCMP0123 = 0X08 / 0X09
PMBUS VCC_CDCORE/VCCMP0123 = 0X43 / 0X44

CAD NOTE:

PLACE PGOOD CAPS CLOSE TO CPLD

PLACE SVID_ALERT SERIES RESISTOR
CLOSE TO VCCD012 VR < 0.5"
SVID TRACE MUST BE NO LONGER
THAN 15" FROM UCCP VR

PULL-UP RESISTORS
SHOULD BE CLOSE TO
VCCD012 VR < 1"

PLACE SVID SERIES RESISTOR
CLOSE TO VCCD012 VR < 0.5"
SVID TRACES MUST BE NO
LONGER THAN 15" FROM UCCP VR

BOM NOTE:

G79911-001 (IR3570B) IS THE BLANK
NON-PROGRAMMED PART, REPLACE WITH
H46348-003 IN BOM

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ROOM: VR_VCC_CDCORE_CONTROLLER

P0V9_VCC_CDCORE/P1V2_VCCMP0123 CONTROLLER

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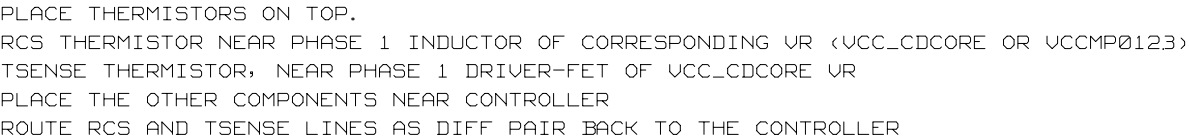
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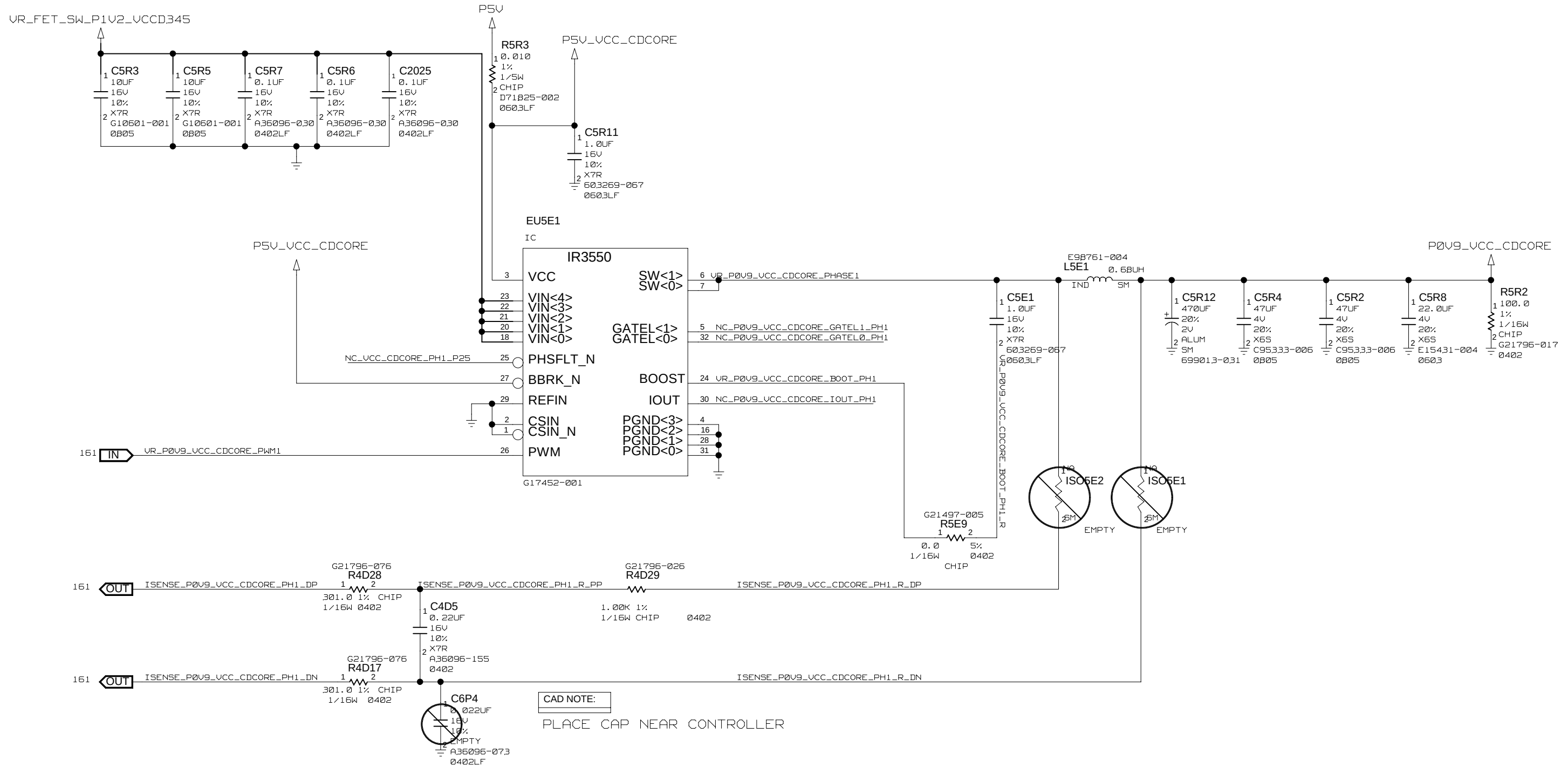
3.13

SCALE:

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ROOM: VCC_CDCORE_PH1

P0V9_VCC_CDCORE PHASE 1

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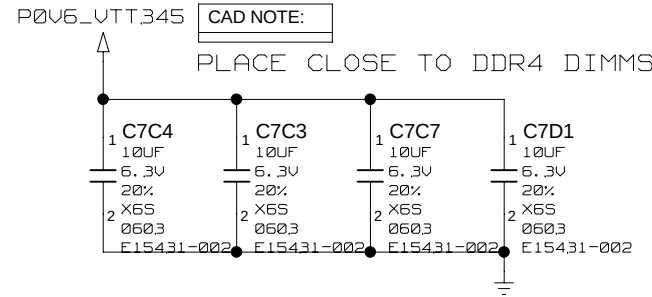
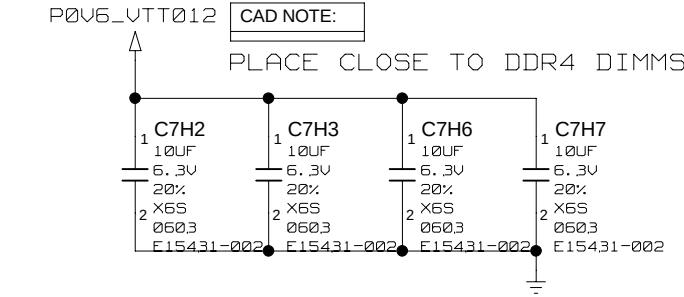
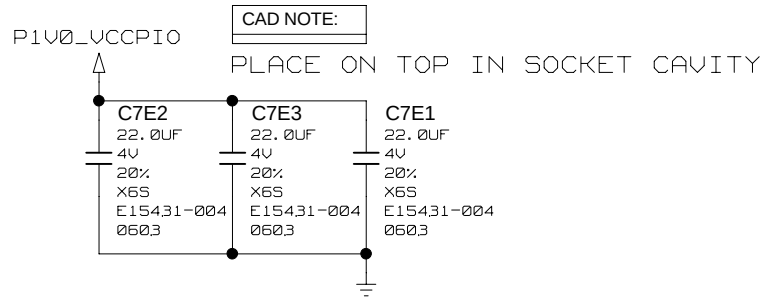
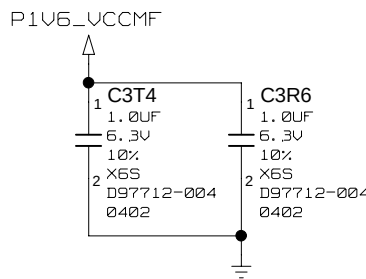
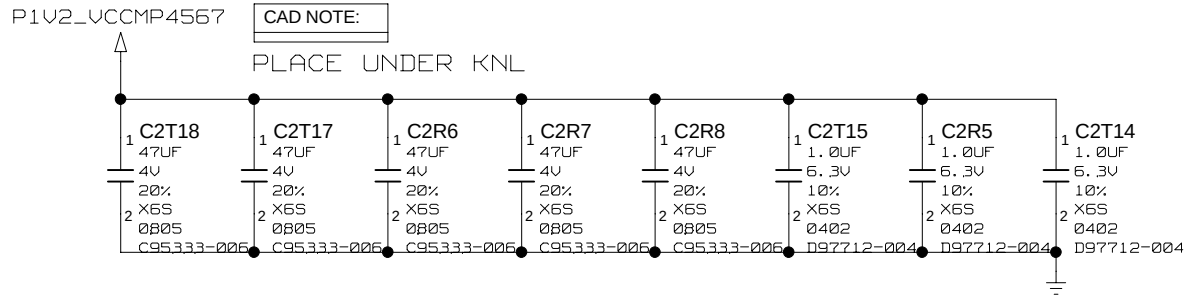
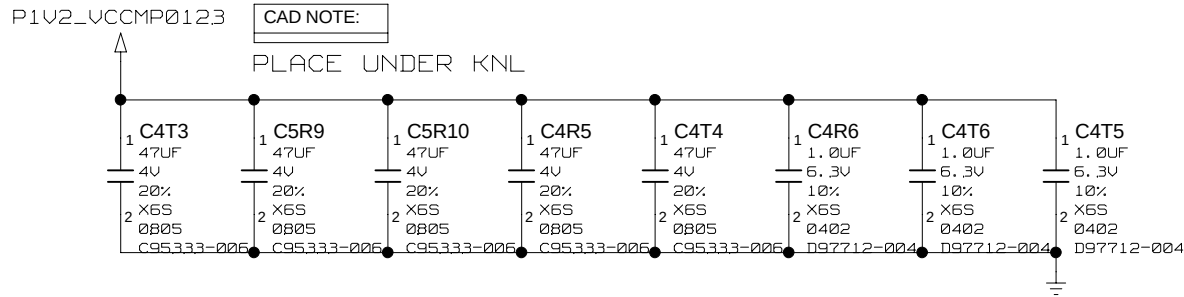
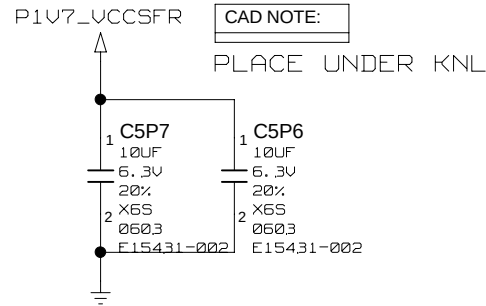
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
CBED	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	G9428608	3.13
SCALE:		DO NOT SCALE DRAWING			SHEET 163 OF 167

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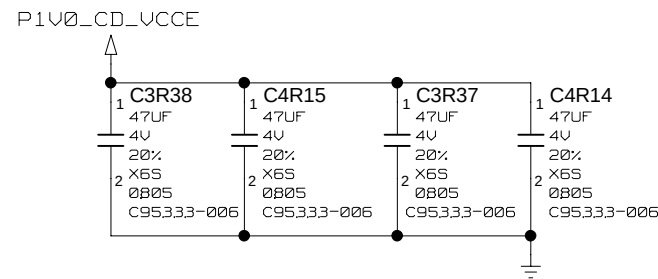
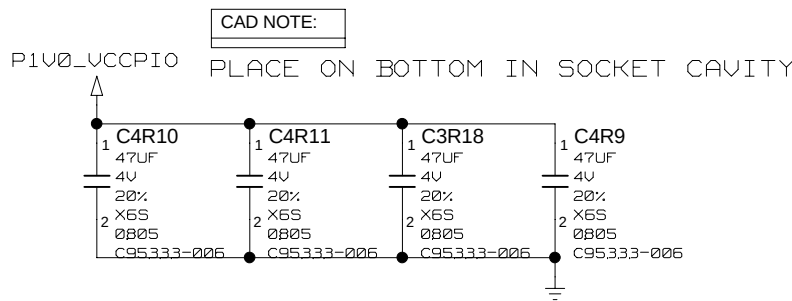
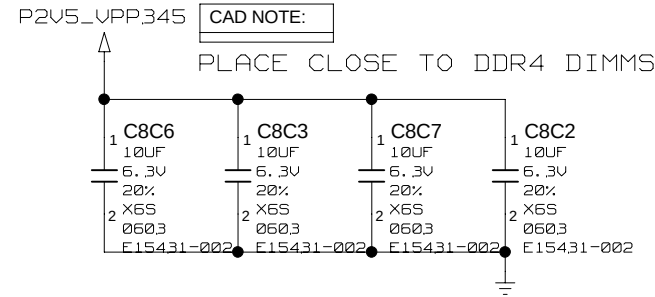
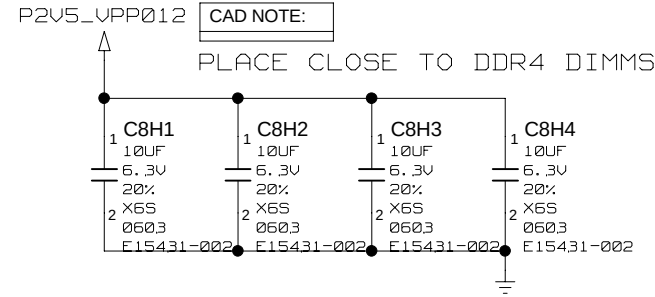
A

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ROOM: DDR4_DIMM_X



ROOM: KNL

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MISC DECOUPLING CAP

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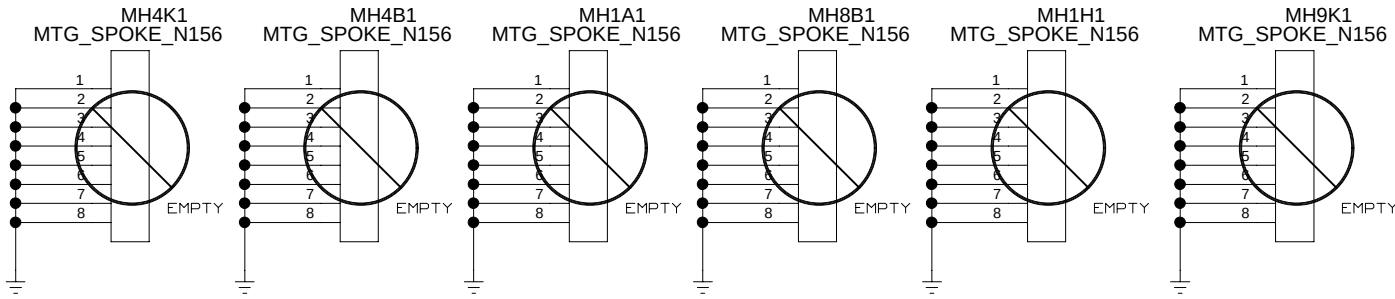
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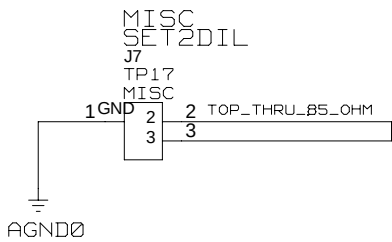
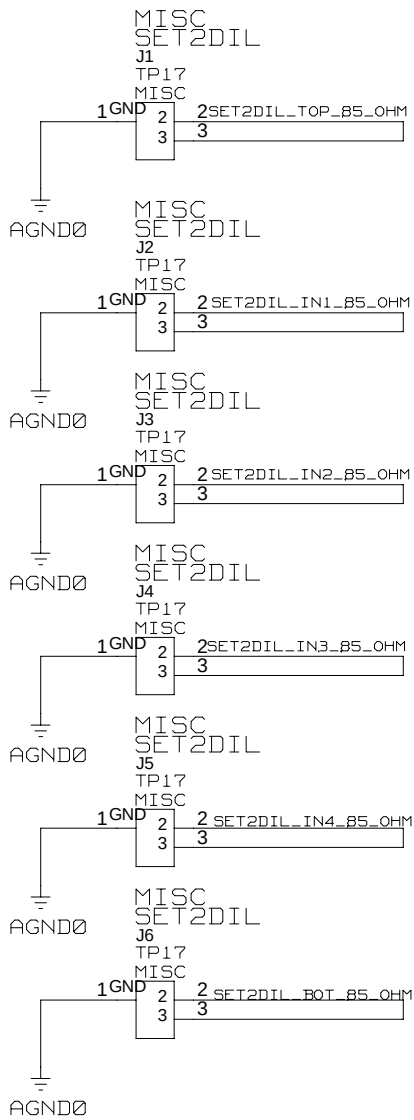
1

CHASSIS MOUNTING HOLES - 156 MIL



SET2DIL

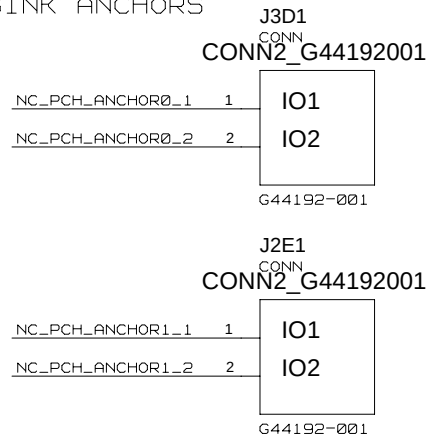
THRU



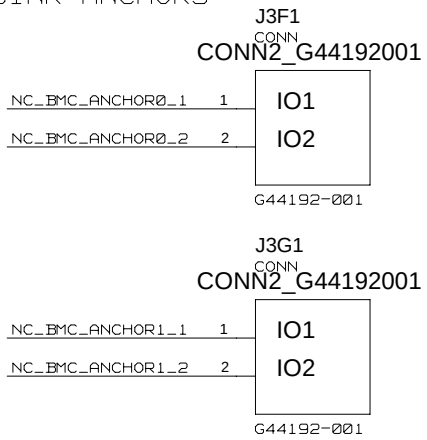
BOM NOTE:

REPLACE SOCKET HALVES
WITH ASSEMBLY
H55975-001 IN BOM

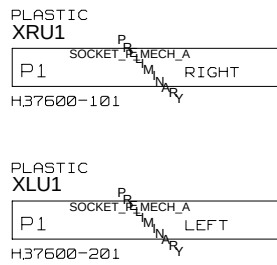
PCH HEATSINK ANCHORS



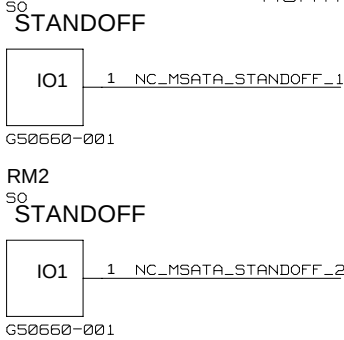
BMC HEATSINK ANCHORS



SOCKET P LEFT & RIGHT HALVES



MSATA STANDOFFS



LB2C1

SNLABEL_A

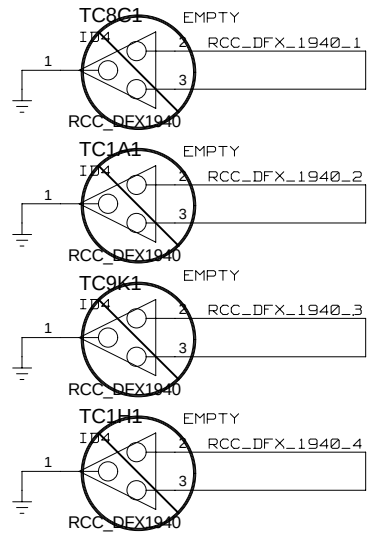
MAC ADDRESS LABEL
IPN A19177-001

ENGINEERING SAMPLE LABEL
IPN=C48561-001

WORK LABEL
IPN=622954-001

PBA/SERIAL NUMBER LABEL
IPN=A19177-001

REWORK LABEL
IPN=A19177-001



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MOUNT HOLES / LABELS / COUPONS

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4

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B

A

PLACE ON TOP

ROOM: ICT_TOP

ICT TEST COMPONENTS

PLACE ON BOT

ROOM: ICT_BOT

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		SCALE:		DO NOT SCALE DRAWING	SHEET 166 OF 167	

4

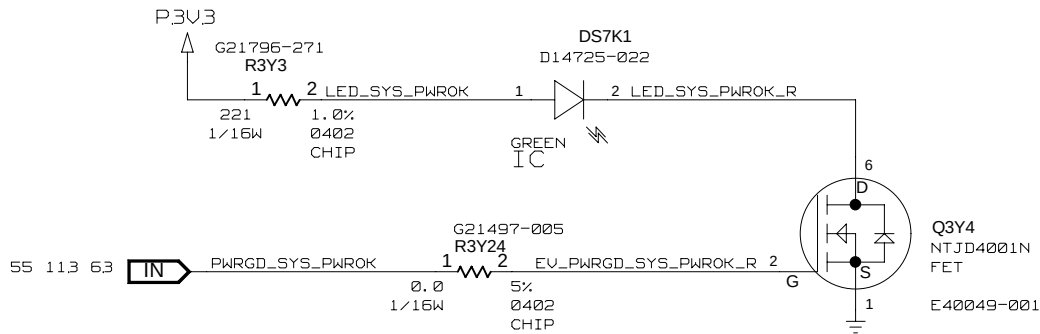
3

2

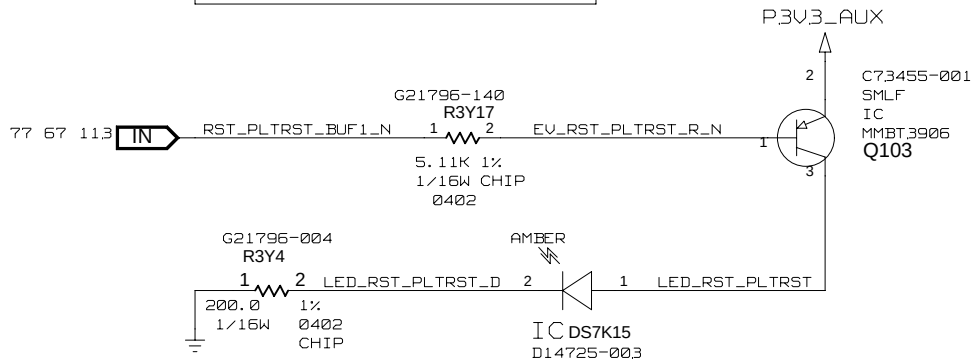
1

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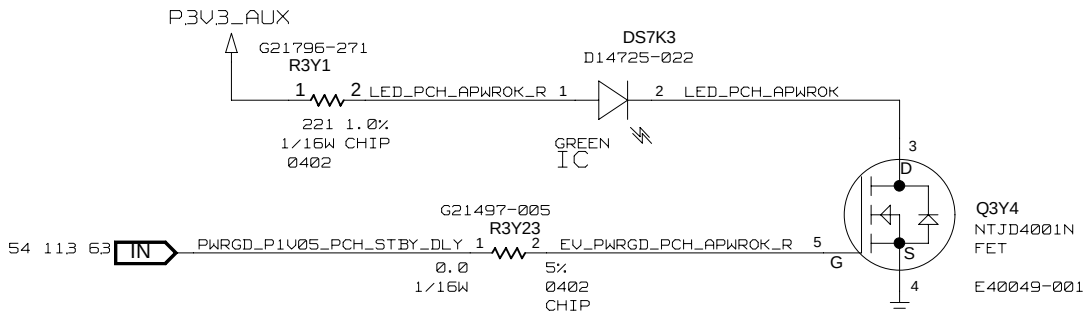
SYS_PWR_OK 1 = ON



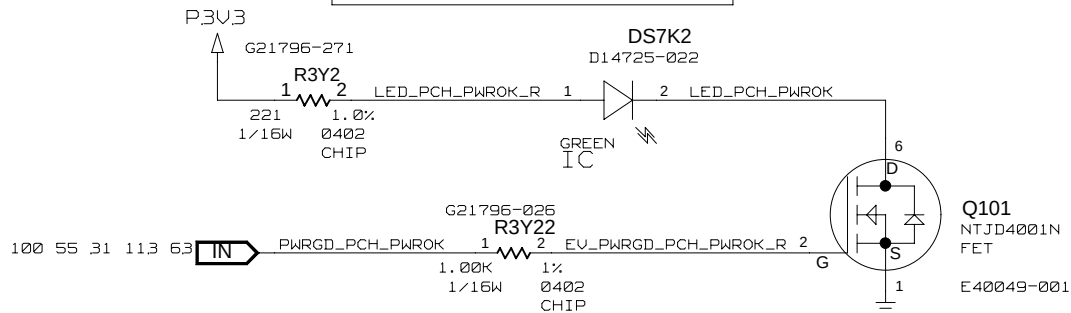
PLT_RST 0 = ON



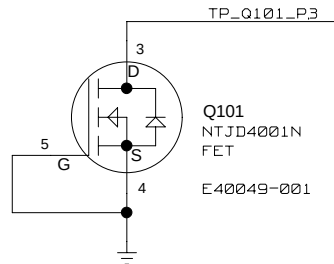
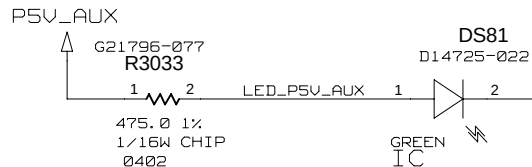
WBG_APWROK 1 = ON



WBG_PWROK 1 = ON



P5V_AUX



ROOM = EV_SYS_DBG_LEDS

SYSTEM RESET LEDES

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